Paper

Nonlinear Dead Beat Control for Boost Converter

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Digital control enable designing of fast responding controllers, useful in nonlinear control. This paper proposes a nonlinear dead beat controller for a boost converter. The controller utilizes the quick reference tracking in finite sampling periods of the dead beat control. Theoretical background is followed by simulations to verify the nonlinear dead beat control algorithm. The simulation is done using the power electronics simulation software (PSIM) on a boost converter rated at mid-range to high power levels. For the purposes of this research the converter was limited to supply a 100 W resistive load.

Keywords: Nonlinear dead beat control, boost converter.

1. Introduction

Boost converters can be easily controlled by digital control methods. [1][2] Such methods are useful for low power converters [1][6] and high power choppers. [3][4] The methods can applied continuous time analysis at the expense of discretizing the control during the experiments as in [3][4].

Digital control is becoming cheaper thanks to re-usability of the same digital hardware to upgrade or change the control. [2][5] The current paper develops a sampled (or discrete) data model of boost converter directly. Sampled data model captures the boost converter's nonlinear characteristics. This paper is organized as follows. Section 2 develops the nonlinear dead beat control law and its practical realization. Section 3 covers the simulations procedures. Section 4 concludes the paper and charts future works on the control algorithm.

2. Nonlinear Dead Beat Control Law

This section presents the derivation of nonlinear dead beat control. Figure 1 is used to explain the theory of the nonlinear dead beat control law. Figure 1(a) shows the converter with its proposed control while Fig. 1(b) shows the waveforms related to dead beat control. In Fig. 1(a) $\boldsymbol{E}$ is the input DC voltage, $\boldsymbol{L}$ is the inductance with its series equivalent resistance r_L. i_L is the inductor current taken as continuous conduction mode (CCM) in this paper. $\boldsymbol{C}$ and $\boldsymbol{R}$ make up the output filter capacitor and resistor and v_O is the output voltage.

In dead beat control block the continuous time signals $[i_L(t)\ v_O(t)]^T$ are sampled by the analog to digital converters (A/D) blocks to give the discrete time signals $[i_L[k]\ v_O[k]]^T$. Dead beat control period $T_2[k]$ calculated is sent to the digital pulse width modulator (DPWM) which makes gate driver to switch **ON** or **OFF** the switch of the boost converter. Figure 1(b) shows the PWM pulse $T_2[k]$ applied during the switch **OFF** duration in the middle of the sampling period T_s. $T_2[k]$ is calculated based on time instant kT_s values i.e. $[i_L[k]\ v_O[k]]^T$. The three intervals are taken such that $T_1[k] = T_3[k] = T_{ON}/2$, where T_{ON} is the switch **ON** duration. $T_2[k] = T_{OFF}$ which is the switch **OFF** duration. To derive the dead beat control uses following considerations. The first is that the continuous time signals' gradients do not change within the sampling period. The second is to use the Euler's approximation to estimate the next sampling period discrete signals. Together with the dynamic model of the boost converter [4] yields stacked matrix integral equations with products having higher orders of T_i where {i=1,2,3}. However these T_i {i=1,2,3} are smaller than T_s, then all terms containing products of more than one T_i {i=1,2,3} are ignored since they are smaller than other terms. The boost converter discrete time model is written in equation (1) and (2).

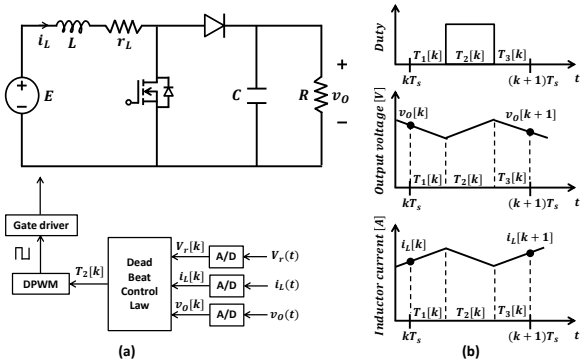


Fig. 1. Boost converter with dead beat control.

$$v_O[k+1] = \left[1 - \frac{T_s}{RC}\right] v_O[k] + \frac{1}{C} i_L[k] T_2[k] \quad \cdots\cdots\cdots (1)$$

$$i_L[k+1] = i_L[k] - \frac{1}{L} v_O[k] T_2[k] + \frac{E}{L} T_s \quad \cdots\cdots\cdots\cdots (2)$$

The aim of the dead beat control is to drive the output voltage $v_O[k+1]$ to reach the reference voltage $V_R[k+1]$ in finite sampling time. Therefore replacing $v_O[k+1]$ by $V_R[k+1]$ in equation (1) leads to equation (3), the nonlinear dead beat control law.

$$T_2[k] = \frac{V_R[k+1] - \left[1 - \frac{T_s}{RC}\right] v_O[k]}{\frac{1}{C} i_L[k]} \quad \cdots\cdots\cdots\cdots (3)$$

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Table 1. Boost Converter Parameters.

Parameter name	Value	Units
Inductance L	5.5	μH
Capacitance C	100	μF
Rated load (100%) R	1.41	Ω
Rated input DC voltage E	12 – 14	V

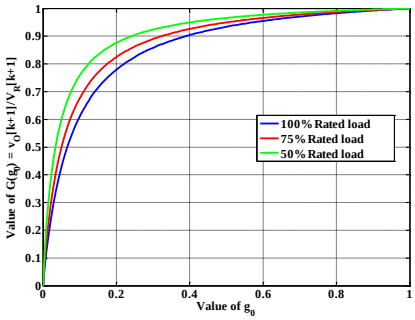


Fig. 2. Ratio $v_O[k+1]/V_R[k+1]$ Vs g_0 in equation (5).

Substitution into (1) and (2) of equation (3) will show that $v_O[k+1]$ approaches $V_R[k+1]$. Further $i_L[k+1]$ approaches $V_R[k+1]/(R(1-D))$ where $\boldsymbol{D}$ is the steady state duty ratio of the converter.

However control law developed in equation (3) has serious practical limitations when the current $i_L[k]$ is too small close to the discontinuous conduction mode (DCM). The dead beat control period $T_2[k]$ becomes too large and saturates the DPWM causing long switch **OFF** duration, the converter goes into DCM. This can be avoided by multiplying equation (3) with a small gain $g_0 = [0,1]$ to ensure that $T_2[k]$ stays within limits of T_s. The new dead beat control period will be $T_2^{new}[k] = g_0 T_2[k]$ given in equation (4).

$$T_2^{new}[k] = g_0 \frac{V_R[k+1] - \left[1 - \frac{T_s}{RC}\right] v_O[k]}{\frac{1}{C} i_L[k]} \quad \cdots\cdots\cdots (4)$$

At steady state, when $k \to \infty$, $v_O[k] \approx v_O[k+1]$. Equation (4) is substituted into equation (1). Ratio of output voltage to its reference is $G(g_0) \equiv v_O[k+1]/V_R[k+1]$ written as equation (5).

$$G(g_0) = \frac{g_0}{1 - \left[1 - \frac{T_s}{RC}\right][1 - g_0]} \quad \cdots\cdots\cdots\cdots\cdots (5)$$

This ratio estimates how much the actual voltage will be close to the reference voltage. Table 1 lists the parameters of the converter used in this study. The load resistor value listed in Table 1 is the one drawing rated load current (100%) at the rated output voltage of 30 V. Figure 2 shows the theoretical prediction of equation (5) with different load condition. It shows that it is possible for the output voltage to track the reference by more than 90% by selecting g_0 around 0.4 or above.

At steady state, when $v_O[k+1] = V_R[k+1]$, the gain g_0 is calculated by equation (6)

$$g_0 = [1 - D] \frac{R I_{Lss}}{V_{Oss}} \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (6)$$

where I_{Lss} and V_{Oss} are the steady state inductor current and output voltage respectively.

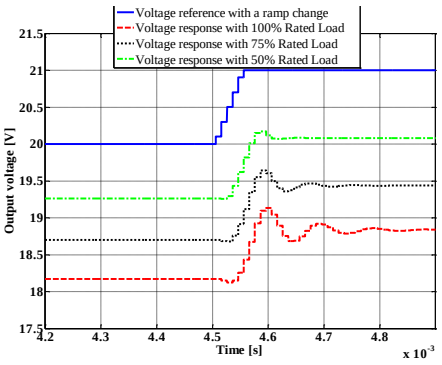


Fig. 3. Output voltage simulation results at $g_0 = 0.4$.

3. Simulation

This section presents the simulation procedures and results. The nonlinear dead beat control law is applied to a switching model of boost converter built on power electronics simulation software (PSIM). The model is a virtual emulation of the actual experimental setup. The AD blocks are provided by the inbuilt library blocks. The PWM pulse is generated after comparison of control signal with a triangle carrier of ±1 V. Sampling period and switching periods are 10 μs.

Figure 3 shows the simulation results of output voltage reference V_R and responses v_0. The figure shows that before 4.5 ms, the voltage reference is 20 V. Thereafter a reference ramp of 1 V is applied for duration of 50 μs. The figure confirms the prediction of equation (5) as well as that the response tracks the reference within few sampling periods.

4. Conclusion

This paper has proposed a nonlinear dead beat control for boost converter. Conditions for practical implementation have been derived and the control algorithm was applied to the converter. Simulation results show that the control is able to track the reference changes within few sampling periods. Further work to to improve the results is being undertaken. Experimental verification will be reported in future publication.

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