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Paper

Fast and Robust Nonlinear Deadbeat Current Control for Boost Converter

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This paper proposes a fast and robust nonlinear deadbeat control for boost DC–DC converters. First, the nonlinear state equation is derived, and second a nonlinear current reference deadbeat control is proposed. Third, a new nonlinear controller to implement the load disturbance compensation is proposed. After the simulations and verification by experiments, it was confirmed that under the conditions of an input voltage of 12 V, an output voltage of 20 V, a load resistance of 4 Ω and a sampling frequency of 100 kHz, the voltage command tracking capability of a settling time of 280 μs was achieved, and an output voltage recovery time of 1.46 ms was achieved for a sudden load change.

Keywords: boost converter, digital control, deadbeat control, disturbance observer, settling time, recovery time

1. Introduction

The performance of DC–DC converters may be evaluated by two kinds of performance index: (1) the command voltage tracking capability and (2) robustness to the disturbances [1]. Among several DC–DC converters, the boost type has an unstable zero in the plant, thus it is said to have difficulties in higher performance. Based on the literature survey on boost type converters, Shirazi et al. [1] proposed an online tuning control based on the system-identification algorithm called PRBS (pseudo random binary sequence) perturbation [2]. After the plant parameters are identified online, a digital PID controller regulates the output voltage. It was reported that under the conditions of the input voltage 15 V, output voltage 30 V load resistor 100 Ω, and sampling frequency 195 kHz, the voltage command tracking capability is 800 μs settling time and the output voltage recovery time is 0.6 ms after load change. Another literature Tong et al. [3] reported sensorless predictive peak current control, in which a minor current deadbeat controller is employed based on the state space average model using the estimated current and the digital PID control regulated the output voltage. It was reported that under 5 V input voltage, output voltage 15 V, 10 Ω load resistor and 100 kHz sampling frequency, the input voltage was abruptly changed from 5 V to 6 V and the output voltage dip recovered within 0.18 ms. However the output voltage tracking command capability was not mentioned at all and the related references [4]–[6] indicated a few ms settling time for the voltage command. Other literatures will be summarized in the Section 4. However it seems that these two literatures [1][3] have the best records at this moment.

Reference [7] proposed nonlinear deadbeat current control for a buck converter and resulted into faster and robust dynamics. Authors propose a new discrete time domain nonlinear state equation and nonlinear deadbeat control for a boost converter with a current minor loop. The load current observer is also implemented aiming the disturbance robustness based on this modeling. As a result under the conditions of input voltage 12 V, output voltage 20 V, the load resistor 4 Ω and 100 kHz sampling frequency, the voltage command tracking capability of 280 μs settling time was confirmed, and also 1.46 ms output voltage recovery time was experimentally achieved for a sudden load change. These data seem among the best even though the proposed control is based on nonlinear equations.

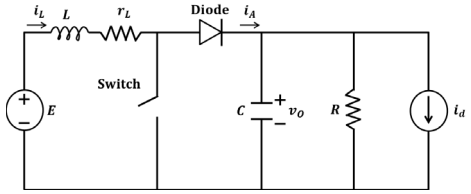

Fig. 1. Boost converter equivalent circuit

In Section 2 of this paper the control scheme of nonlinear deadbeat control is described and consequent several kinds of control law are proposed, and the Section 3 shows the simulations and the experiments. The features of this proposed control are discussed with comparison of other literatures in the Section 4, and the Section 5 concludes this paper. Several mathematical calculations are summarized in Appendix.

2. Theory of Nonlinear Deadbeat Control for Boost Converter

This section presents the theoretical framework of the nonlinear deadbeat control for the boost converter. The nonlinear state equation is first derived, [8] and second a nonlinear current reference deadbeat control [7] is proposed. Third, the load disturbance compensation is implemented, and as a final result, a new nonlinear controller is proposed as shown in Fig. 4.

2.1 Basic Definitions for Digital Control Figure 1 shows the equivalent circuit of a boost converter. Input voltage is E, inductance is L, current through inductor is $i_L(t)$, and inductor leakage resistance is r_L. The output capacitor is

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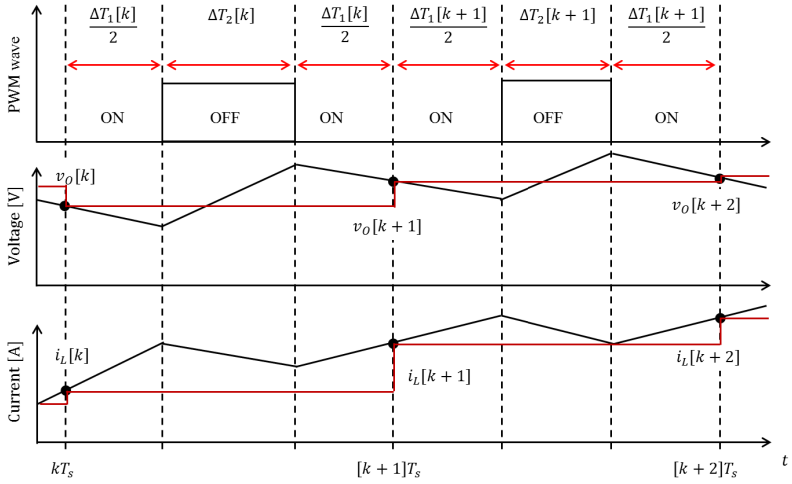

Fig. 2. Deadbeat control waveforms: black – actual waveform, red – sampled waveform

C, output load resistor is R and output voltage is $v_O(t)$. The load disturbance is represented by the current source $i_d(t)$ attached at the output. The load R and disturbance $i_d(t)$ have been differentiated to simplify the derivation of the nonlinear deadbeat control law, discussed later. The total output load current is represented by $i_A(t)$ and is made up of current through R, C and $i_d(t)$. The t in the brackets symbolizes continuous time index.

The derivation is done according to the waveforms presented in Fig. 2. The $\Delta T_1[k]$ and $\Delta T_2[k]$ are ON and OFF times of the switch respectively. The sampling period is given as $T_s = \Delta T_1[k] + \Delta T_2[k]$. The pulse width duration $\Delta T_2[k]$ is placed at the center of the sampling period. The k in the square brackets symbolizes the discrete time index. Voltage and current sampled signals are presented by the red curves.

2.2 Sampled Data Nonlinear Model The derivation of sampled data nonlinear model of the boost converter was summarized in Appendix 1, [8] and the derived sampled data nonlinear equations are shown in (1) and (2) considering the case of continuous conduction mode (CCM).

$$v_O[k+1] = \left(1 - \frac{T_s}{RC}\right) v_O[k] + \frac{1}{C} i_L[k]\Delta T_2[k] - \frac{T_s}{C} i_d[k] \quad \cdots\cdots (1)$$

$$i_L[k+1] = \left(1 - \frac{r_L}{L} T_s\right) i_L[k] - \frac{1}{L} v_O[k]\Delta T_2[k] + \frac{T_s}{L} E \quad \cdots\cdots (2)$$

Where $v_O[k]$, $i_L[k]$, and $i_d[k]$ represent output voltage, inductor current, and disturbance current at instant k. The equations are nonlinear especially $i_L[k]\Delta T_2[k]$ in (1) and $v_O[k]\Delta T_2[k]$ in (2) show very strong bilinear characteristics. However, due to use of the digital control the nonlinear deadbeat control is proposed in the next Section.

2.3 Nonlinear Current Reference Deadbeat Control for Boost Converter [7] In the previous study [8] the voltage equation (1) was used to develop the nonlinear deadbeat controller. But it suffered from the fact that the duty ratio saturated for high gain parameters and the output voltage was oscillatory, as a result a very slow response was realized. Due to the nonminimum phase nature of boost converter, a sudden change of duty ratio causes an inverse response, and this also has influence to this slow response. The saturation of the duty ratio is mainly due to the large current in the switching device. Thus the inductance current is directly controlled by a new approach "current reference deadbeat control" [7]. In this paper this concept is modified for boost converter. Using (2) and changing the $i_L[k+1]$ to reference current $I_{ref}[k+1]$, the new control law "current reference nonlinear deadbeat" law is proposed in (3).

$$\Delta T_2[k] = \frac{\left(1 - \frac{r_L}{L} T_s\right) i_L[k] - I_{ref}[k+1] + \frac{E}{L} T_s}{\frac{1}{L} v_O[k]} \quad \cdots\cdots (3)$$

The feature of this control is how to determine one sampling ahead current reference $I_{ref}[k+1]$, the selection of which is very important because this value enables the very quick response under the current limit of the switching device.

The current reference [7] is decided as shown in (4).

$$I_{ref}[k+1] = A\left(v_{ref}[k+1] - v_O[k]\right) + I_{Lave}[k] \cdots\cdots (4)$$

The first term is based on the output voltage error which is the difference of the voltage reference $v_{ref}[k+1]$ at the time $k+1$ and the actual output voltage $v_O[k]$ at time k and this term regulates the output voltage. The second term $I_{Lave}[k]$ is a steady state inductance current at time k. These two terms will be discussed in the next sections.

2.3.1 Selection of A in (4) The energy at the capacitor C in Fig. 1 should be increased when the voltage changes from $v_O[k]$ to $v_{ref}[k+1]$, and this energy increase should be supplied from the stored energy at inductor L. Thus, following equation may be approximately assumed.

$$\frac{1}{2} L I_{ref}^2[k+1] \frac{\Delta T_2[k]}{T_s} \approx \frac{1}{2} C \left(v_{ref}[k+1] - v_O[k]\right)^2 \cdots\cdots (5)$$

Solving this for $I_{ref}[k+1]$ yields,

$$I_{ref}[k+1] \approx \sqrt{\left(\frac{C}{L}\right)\left(\frac{T_s}{\Delta T_2[k]}\right)} \left(v_{ref}[k+1] - v_O[k]\right). \quad \cdots\cdots (6)$$

Comparing (4) and (6), A may be given as in (7).

$$A \approx \sqrt{\left(\frac{C}{L}\right)\left(\frac{T_s}{\Delta T_2[k]}\right)} \quad \cdots\cdots (7)$$

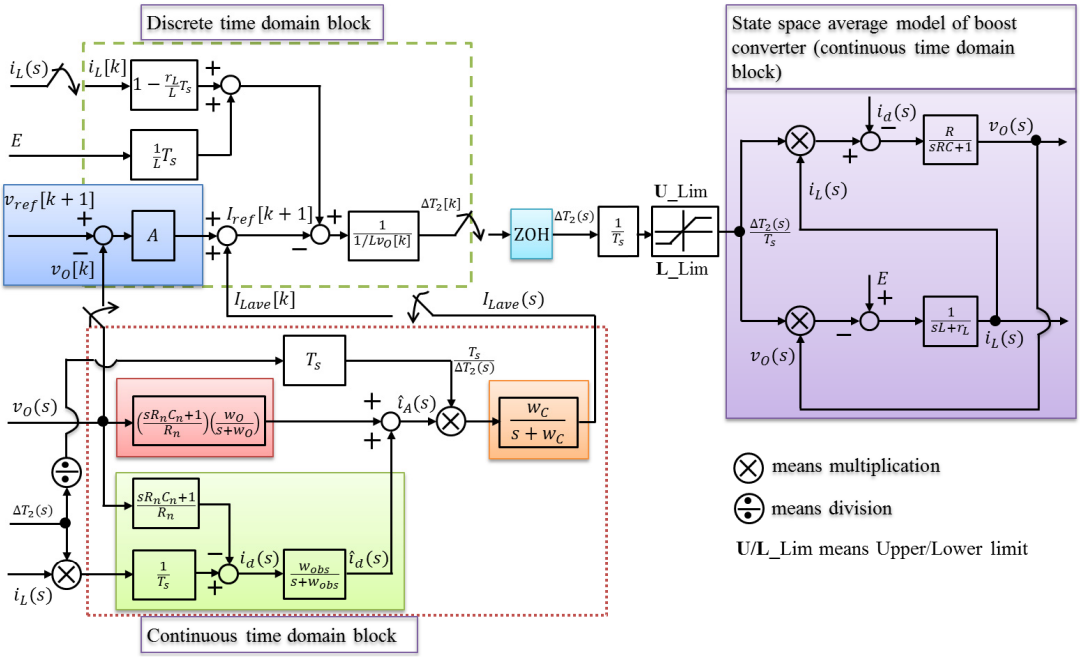

Fig. 3. Proposed nonlinear deadbeat control block diagram including disturbance observer

The actual selection of A is done by trial and error during the simulation and experiment because this explanation is based on very rough assumption. However, (7) gives a range of selection of A.

2.3.2 Selection of $I_{Lave}(s)$ in (4) The derivation of transfer function of output voltage $v_O(s)$ and inductor current $i_L(s)$ based on the state space averaging method is summarized in Appendix 2. The derived plant model is shown in Fig. 3, which has two kinds of blocks, (1) discrete time domain block, and (2) continuous time domain block. In the time domain block, assuming the disturbance $i_d(s) = 0$, then the averaging output current $i_A(s)$ is obtained as an inverse system of the plant, as follows:

$$i_A(s) = \frac{sR_nC_n + 1}{R_n} v_O(s) \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (8)$$

This estimated output $i_A(s)$ has a derivative component, and should be low pass filtered as follows.

$$\hat{i}_A(s) = \frac{w_O}{s + w_O} i_A(s) \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (9)$$

Then the inductance average current $I_{Lave}(s)$ is proportional to $T_s/\Delta T_2(s)$, but $\Delta T_2(s)$ has high frequency components, thus it should go through LPF as follows,

$$I_{Lave}(s) = \left(\frac{w_C}{s + w_C}\right)\left(\frac{T_s}{\Delta T_2(s)}\right)\hat{i}_A(s). \cdots\cdots\cdots\cdots (10)$$

This is a kind of nonlinear filter as shown in Fig. 3, and this is one of unique features of this control law. The selection w_O and w_C is as follows. w_O is the cut-off frequency of the load current smoothing effect, thus it should be a little lower than the LC filter. w_C is the cut-off frequency of the duty cycle averaging, thus it should be selected based on the switching frequency and the disturbance rejection as discussed later. Actual digital realization of (10) is done by Tustin transformation as summarized in Appendix 3.

2.3.3 Suppression of Disturbance When a sudden change of load happens, the output voltage drops for a while and the output voltage recovers to the reference voltage depending on the voltage regulator control. This period is defined as a recovery time and for shortening this time, a new disturbance observer is proposed. In Section 2.3.2 the average load current was estimated, however, a disturbance current has higher frequency components and can be estimated by a disturbance observer and feed forward the estimated current to the second term in (4). The plant model is again based on the state space averaging model as shown in Appendix 2, thus the block in Fig. 3 is applicable. The estimated disturbance $\hat{i}_d(s)$ becomes,

$$\hat{i}_d(s) = \frac{w_{obs}}{s + w_{obs}}\left(\frac{\Delta T_2(s)}{T_s} i_L(s) - \frac{sR_nC_n + 1}{R_n} v_O(s)\right). \cdots\cdots\cdots\cdots\cdots (11)$$

In above computation R_n and C_n are nominal parameters and they are usually a little different from the plant parameters shown in Fig. 3. This signal is added to the $\hat{i}_A(s)$ in (9) and it becomes,

$$\hat{i}_A(s) = \frac{w_O}{s + w_O} i_A(s) + \hat{i}_d(s). \cdots\cdots\cdots\cdots\cdots\cdots (12)$$

This new $\hat{i}_A(s)$ should be low pass filtered by (10). The derived disturbance suppression is shown in Fig. 3.

2.3.4 Overall Control Block Diagram and Free Parameters The derived overall control law is summarized in Fig. 3, in which digital control and analogue control are drawn together, however, analogue control is actually realized digitally by Tustin transformation as shown in Appendix 3. The left hand upper block is the nonlinear deadbeat part, and the left hand lower block is responded to the disturbance observer, and the right hand block is the plant.

There are several free parameters in Fig. 3, which are (1) load current observer cut-off frequency w_O, (2) boost converter switching frequency smoothing filter frequency w_C,

and (3) disturbance observer cut-off frequency w_{obs}. The $I_{ref}[k+1]$ gain A is also a little changeable.

3. Simulations and Experiments

This section presents the simulations and experiments conducted in verification of the proposed nonlinear current reference deadbeat control law for boost converter.

Simulations were done using the power electronics simulations software (PSIM). Conditions and circuit components values are summarized in Table 1.

Experiments were done on the boost converter with parameters from Table 1 using a digital control system with a floating point digital signal processor (DSP) TMS320F28335. Current measurements were obtained using LEM CAS 15–NP sensor. Voltage measurements were obtained using a voltage divider bridge. Voltage command was changed on the computer keyboard while the disturbance was connected by a digital circuit to the output of the converter.

3.1 Voltage Reference Tracking The voltage reference was abruptly changed from 14.64 V to 20.0 V. Simulated voltage command tracking capability results are presented in Fig. 4 while experiment verification of voltage command tracking capability results are presented in Fig. 5.

Table 1. Boost Converter Parameters

Parameter	Symbol	Value	Units
Inductance	L	22	μH
Inductor ESR	r_L	0.05	Ω
Capacitance	C	60	μF
Resistor load	R	4	Ω
Input DC voltage	E	12	V
Switching frequency	f_s	100	kHz
Sampling period	T_s	10	μs

Performance index measured is voltage settling time (t_s) which is defined as the period for the voltage to rise from 0% and stay within 90% of the voltage command. Simulated results (Fig. 4) show settling time 277 μs and experiment results (Fig. 5) show settling time 280 μs. The negative voltage response (from 14.64 V drop to 14.0 V) due to the presence of right-half-plane zero [9][16] is observed. The current responses during the voltage tracking are shown in Fig. 6 for simulation and Fig. 7 for experiments. They show good agreements.

3.2 Disturbance Suppression Load disturbance was input by a sudden connection of unknown resistor bank to the output of the converter. Disturbance suppression capability results are presented in Fig. 8 for simulations and in Fig. 9 for experiments.

Performance index measured is the voltage recovery time (t_{rec}) defined as the period for the voltage to recover from 100% voltage dip to when about 90% of the voltage dip is recovered for sudden disturbances. Simulated results (in Fig. 8) and experiment results (in Fig. 9) show disturbance suppression capability with recovery time 1.34 ms and 1.46 ms respectively.

4. Discussions

This section presents further discussions about the present research and also makes comparison to previous literatures.

4.1 Originality of this Research This paper has

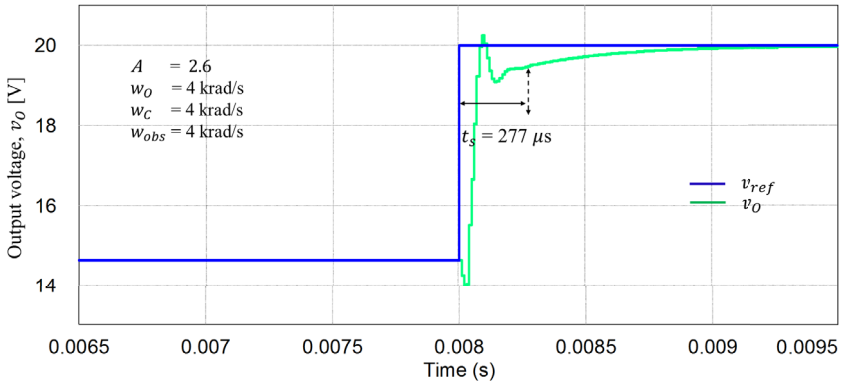

Fig. 4. Output voltage and reference (voltage tracking settling time 277 μs, simulation)

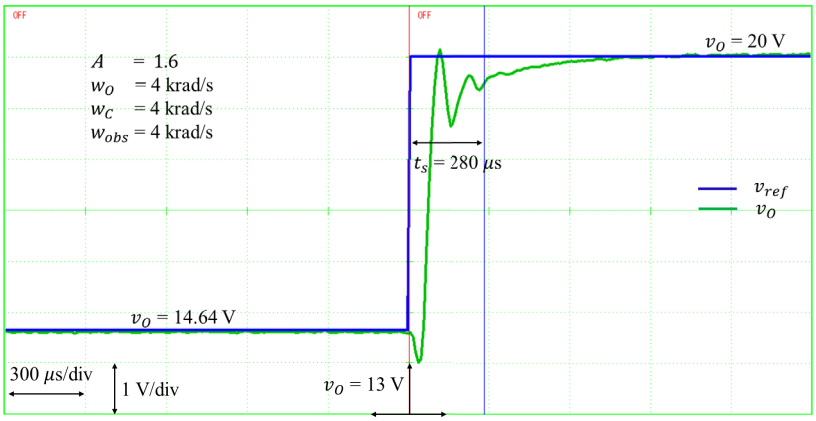

Fig. 5. Output voltage and the reference (voltage tracking settling time 280 μs, experiment)

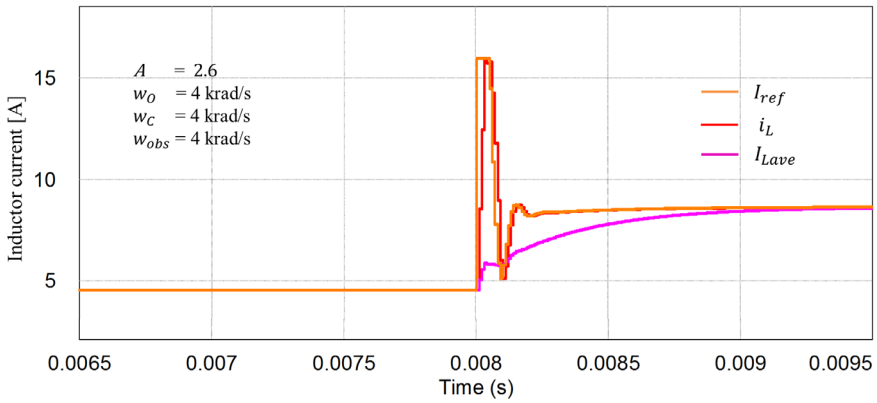

Fig. 6. Inductor currents during voltage tracking (simulations)

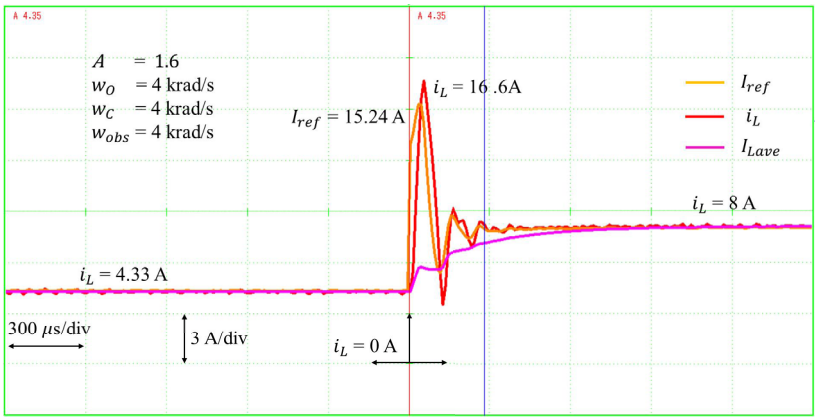

Fig. 7. Inductor currents during voltage tracking (experiments)

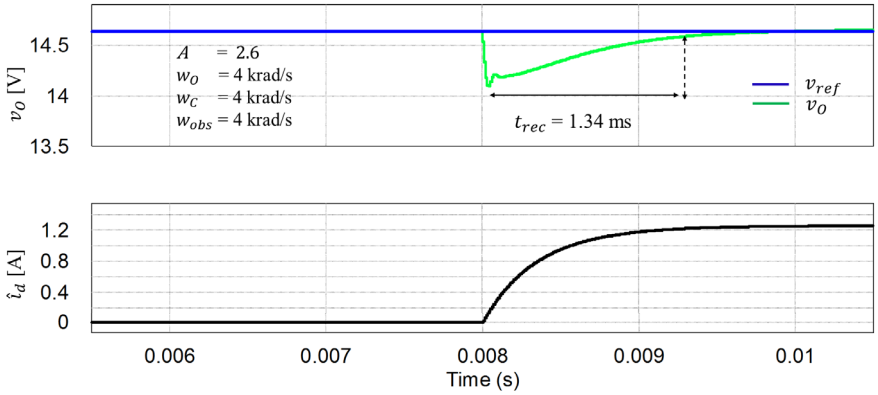

Fig. 8. Upper curves are the output voltage disturbance recovery time 1.34 ms with the reference, bottom curve is the estimated disturbance (simulations)

achieved the following five contributions. Firstly it has developed the discrete time nonlinear state equations for a boost converter. Secondly it has used this modeling to develop a nonlinear current reference deadbeat control for a boost converter. Thirdly the current reference is made of two terms, one of which is the output voltage regulation and the other is the estimated steady state inductance current. Fourth, the load disturbance observer is proposed and it is added to this current reference term for feedforward compensation. Finally a very quick reference voltage tracking was experimentally achieved among other literatures while the disturbance recovery time is still in the reasonably quick range. The selection of the three parameters in Fig. 3 is done as follows. The w_O is the smoothing filter for the average load, and it should be the lowest among w_C and w_{obs}. w_C is the cut-off frequency of the low pass filter for the nonlinear term $T_s/\Delta T_2(s)$. It should be a little higher than w_O. Also w_{obs} is the cut-off frequency of the load disturbance observer, thus it should be high enough to compensate the high frequency disturbance components. As a result following conditions may be reasonable.

$$w_O < w_C, w_O < w_{obs}, w_C \leq w_{obs} \cdots\cdots\cdots\cdots\cdots\cdots (13)$$

This suggestion can be confirmed in Figs. 10 and 11. Use of (7) to calculate gain A is possible in simulations, but authors found that due to square root and inverse operation involved,

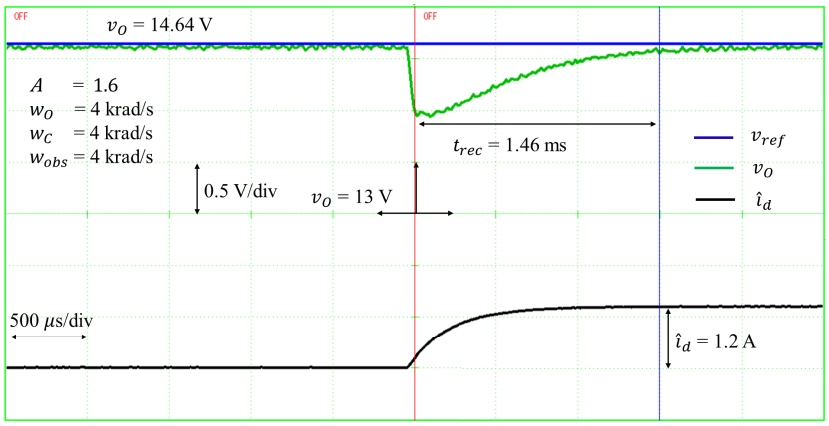

Fig. 9. Upper curves are the output voltage disturbance recovery time 1.46 ms with the reference, bottom curve is the estimated disturbance (experiment)

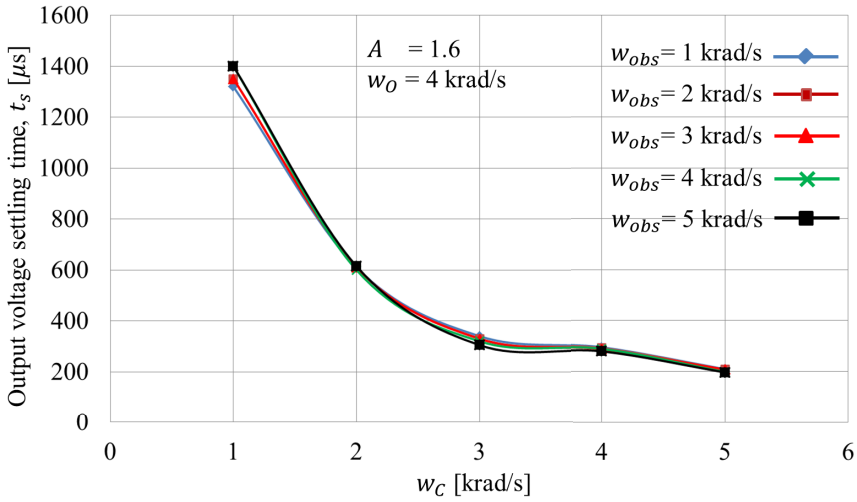

Fig. 10. Experiment results of settling time (t_s) trends

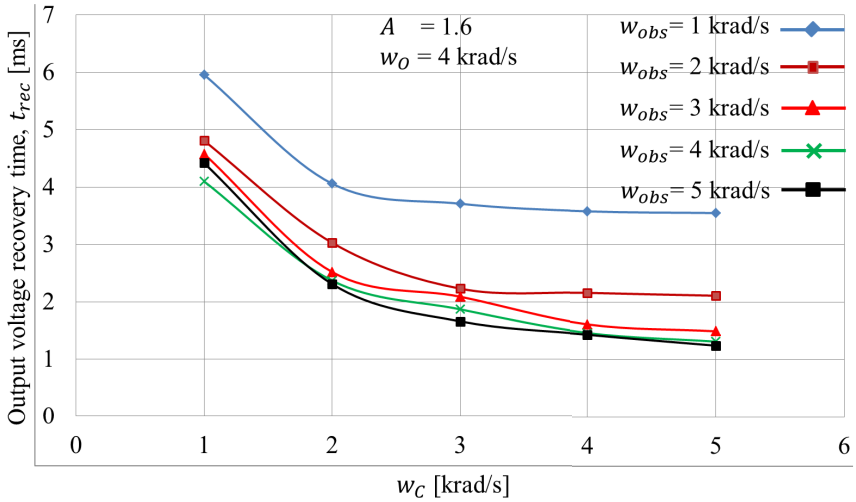

Fig. 11. Experiment results of recovery time (t_{rec}) trends

it became unstable during experiment DSP implementation. Thus they chose constant gain A (A = 1.6 for experiment and A = 2.6 for simulations). Choosing w_O = 4 krad/s investigations of effects of different disturbance observation filters (1.0 ≤ w_{obs} ≤ 5.0 krad/s) and different inductor current estimation filters (1.0 ≤ w_C ≤ 5.0 krad/s) were carried out experimentally. Gain A for simulation is higher, because there is no delay in control during simulation, while in experiment there is control delay and when gain A is large it causes large output voltage oscillations. That is why gain A was determined experimentally lower than for simulation. Summary of the results is presented in Figs. 10–11.

Due to condition in (13) and arrangements of Fig. 3, w_C has higher influence on the settling time than does w_{obs}. It should

Table 2. Performance Comparison with Past Literatures of Digital Control Methods on Boost Converters

Authors	Switching frequency [kHz]	Sampling period [μs]	Input voltage [V]	Output voltage change [V]	t_s [μs]	Disturbance (load change)	t_{rec} [ms]
Flores et al., 2014 [11]	45	100	NA**	15 → 24	3000	89 → 38 Ω	Not known*
Oucheriah et al., 2013 [12]	200	NA**	6 → 10	7 → 12	25000	160 → 40 Ω	20
Tong et al., 2014 [3]	100	10	5 → 6	15	NA**	15 → 10 Ω	0.18
Karamanakos et al., 2014 [13]	NA**	10	10 → 15	15 → 30	1900	73 → 36.5 Ω	0.7
Oettmeier et al., 2009 [14]	16	NA**	115	165 → 175	1700	NA**	NA**
Shirazi et al., 2009 [1]	195	0.72	15	30 → 35	800	0.3 → 0.6 A	0.6
Chen et al., 2011 [9]	20	1	20	35 → 40	10000	40 → 30 Ω	10
Takei et al., 2014 [15]	10	NA**	50	100	NA**	3 → 8 A	5
Mushi et al., 2015 [16]	100	10	12	20 → 21	5000	2 → 2.5 A	17
This paper	100	10	12	14.64 → 20.0	280	4 → 3 Ω	1.46

t_s is the settling time defined as period for the voltage to change from 0% of command voltage to its settling value within 90% command voltage.

t_{rec} is the recovery time defined as period for the voltage to recover from 100% voltage dip to when more than 90% of the voltage dip is recovered after sudden disturbance.

Not known*	Difficult to read data from figure presented in that paper.
NA**	Figure and/or data not available in that paper.
→	Means from to.

be noted that if w_C is selected very low, the immediate effect is slower voltage responses, see Fig. 10 on left hand side.

Sudden disturbance requires both quick estimation (by w_{obs}) and fast feed forward (by w_C). That is why Fig. 11 shows the disturbance rejection capability increases with increase of both w_{obs} and w_C. In that figure it is noted that if these two filters are fast for example $w_{obs} = w_C = 5.0$ krad/s a 1.2 ms recovery time is realized which is reasonably fast, however it would cause a large overshoot and large oscillations.

4.2 Simplified Stability Explanation The detailed stability analysis is beyond the scope of this paper. However a simplified explanation may be as follows. Putting $\Delta T_2[k]$ in (3) and $I_{ref}[k+1]$ in (4) into (2) yields,

$$i_L[k+1] = I_{ref}[k+1]. \cdots (14)$$

Next, putting (3), (4) and (14) into (1) under the assumption $i_d[k] = 0$ yields,

$$v_O[k+1] = \left(1 - \frac{T_s}{RC}\right) v_O[k] + \frac{T_s}{C} i_L[k] \left(\frac{E - r_L i_L[k]}{v_O[k]}\right). \cdots (15)$$

Under the steady state point, (4) and (14) imply that

$$I_{ref}[k]_{k=\infty} = I_{Lave\infty}. \cdots (16)$$

Also the steady state output voltage is defined as

$$v_O[k]_{k=\infty} = V_\infty. \cdots (17)$$

Putting (16) and (17) into (15) under the assumption that there is an equilibrium point yields,

$$\frac{1}{R} V_\infty = I_{Lave\infty} \left(\frac{E - r_L I_{Lave\infty}}{V_\infty}\right). \cdots (18)$$

Assuming a small perturbation voltage around the equilibrium point as,

$$v_O[k] = V_\infty + \Delta v_O[k], \cdots (19)$$

$$v_O[k+1] = V_\infty + \Delta v_O[k+1]. \cdots (20)$$

Putting (19) and (20) into (15) and using (18) under the assumption that current $i_L[k]$ is constant $I_{Lave\infty}$, and the next approximation is acceptable $\frac{1}{v_O[k]} \approx \frac{1}{V_\infty}\left(1 - \frac{\Delta v_O[k]}{V_\infty}\right)$, then the following will be derived

$$\Delta v_O[k+1] = \left(1 - \frac{2T_s}{RC}\right) \Delta v_O[k]. \cdots (21)$$

This can be solved as

$$\Delta v_O[k] = \left(1 - \frac{2T_s}{RC}\right)^k \Delta v_O[0]. \cdots (22)$$

The value of $(1 - 2T_s/(RC))^k$ is very small as $k \to \infty$, thus $\Delta v_O[k]$ will converge to zero. This is a simplified explanation of stability of the controller. See Appendix 4 for the possible reason of transient oscillations in Figs. 4 and 5.

4.3 Performance Comparisons to Past Literatures The proposed control method is compared to past literatures [1][3][9]–[16]. as shown in Table 2.

Voltage command tracking capability is shown in Table 2 on sixth column (settling time, t_s). Shirazi et al. [1] showed the settling time 800 μs for switching mode power supplies. Oettmeier et al. [14] proposed a model predictive controller (MPC) with a sliding mode observer for portable electronic devices, and reported settling time 1700 μs for voltage change 165 V to 175 V. This paper reports 280 μs settling time for a converter applied in servomotor applications.

Disturbance suppression capability is shown in Table 2 on last column (recovery time, t_{rec}). Tong et al. [3] reported the recovery time 0.18 ms for automotive applications. Karamanakos et al. [13] proposed a direct voltage control using enumeration based MPC for DC motor drives applications, and reported recovery time 0.7 ms for load change 0.2 A to 0.4 A. On the other hand, this paper reports 1.46 ms recovery time for load change 3.66 A to 4.88 A. This load current is 3.6 times larger than that in Tong et al. [3], thus it is in reasonably

quick range.

Comparison with respect to switching frequency is presented in Table 2 on second column. Oucheriah et al. [12] proposed a PWM-based adaptive sliding-mode control for a switching frequency 200 kHz, and reported slower responses than this paper.

Comparison with respect to sampling period is presented in Table 2 on third column. Chen et al. [9] proposed a closed-loop analysis and cascade control for sampling period 1 μs, and reported slower responses than this paper.

It can be concluded that this paper reports better responses than previous literatures.

5. Conclusion

This paper proposes a fast and robust nonlinear deadbeat control for boost DC–DC converters. The nonlinear state equation is first derived, and second a nonlinear current reference deadbeat control is proposed. Thirdly the current reference is made of two terms, one of which is for the output voltage regulation and the other is for the estimated steady state inductance current. Fourthly implementing the load disturbance compensation a new nonlinear controller is proposed. After the verification by simulations and experiments, it was confirmed that under the conditions of input voltage 12 V, output voltage 20 V, the load resistor 4 Ω and 100 kHz sampling frequency, the voltage command tracking capability of 280 μs settling time was achieved, and also 1.46 ms output voltage recovery time was realized for a sudden load change. These data seems the best value among other literatures.

Parameter optimization and the precise stability analysis will be remained for future work.

References

(1) M. Shirazi, R. Zane, and D. Maskimovic: "An Autotuning Digital Controller for DC–DC Power Converters Based on Online Frequency–Response Measurement", *IEEE Trans. Pow. Electron.*, Vol.24, No.11, pp.2578–2588 (2009)

(2) M. Shirazi, R. Zane, D. Maksimovic, L. Corradini, and P. Mattavelli: "Autotuning Techniques for Digitally-Controlled Point-of-load Converters with Wide Range of Capacitive Loads", Proc. IEEE Appl. Power Electron. Conf. 2007, pp.14–20 (2007)

(3) Q. Tong, Q. Zhang, R. Min, X. Zou, Z. Liu, and Z. Chen: "Sensorless Predictive Peak Current Control for Boost Converter Using Comprehensive Compensation Strategy", *IEEE Trans. Ind. Electron.*, Vol.61, No.6, pp.2754–2766 (2014)

(4) J. Chen, A. Prodic, W. Erickson, and D. Maksimovic: "Predictive Digital Current Programmed Control", *IEEE Trans. Power Electron.*, Vol.18, No.1, pp.411–419 (2003)

(5) S. Bibian and H. Jin: "High Performance Predictive Dead-Beat Digital Controller for DC Power Supplies", *IEEE Trans. Power Electron.*, Vol.17, No.3, pp.420–427 (2002)

(6) Y.S. Lai and C.A. Yeh: "Predictive Digital-Controlled Converter with Peak Current-Mode Control and Leading-edge Modulation", *IEEE Trans. Ind. Electron.*, Vol.56, No.6, pp.1854–1863 (2009)

(7) S. Mizushima, A. Kawamura, I. Yuzurihara, A. Takayanagi, and R. Ohma: "Development of DC-DC Converter for High/Low Pulse Voltage Output Using Deadbeat Control", Proc. of IEEE International Future Energy Electronics Conference, IFEEC2015, pp.1–6 (2015)

(8) A. Mushi, S. Nagai, and A. Kawamura: "Nonlinear Dead Beat Control for Boost Converter", Proc. of IEEJ International Workshop on Sensing, Actuation, Motion Control, and Optimization, SAMCON2016, pp.1–2 (2016)

(9) Z. Chen, W. Gao, J. Hu, and X. Ye: "Closed–Loop Analysis and Cascade Control of a Nonminimum Phase Boost Converter", *IEEE Trans. Pow. Electron.*, Vol.26, No.4, pp.1237–1252 (2011)

(10) R.-J. Wai and L.-C. Shih: "Design of Voltage Tracking Control for DC-DC Boost Converter Via Total Sliding–Mode Technique", *IEEE Trans. Industr. Electron.*, Vol.58, No.6, pp.2502–2510 (2011)

(11) J. L.-Flores, A.H. Méndez, C. G.-Rodríguez, and H. S.-Ramírez: "Robust Nonlinear Adaptive Control of a "Boost" Converter via Algebraic Parameter Identification", *IEEE Trans. Industr. Electron.*, Vol.61, No.8, pp.4105–4114 (2014)

(12) S. Oucheriah and L. Guo: "PWM–Based Adaptive Sliding–Mode Control for Boost DC–DC Converters", *IEEE Trans. Industr. Electron.*, Vol.60, No.8, pp.3291–3294 (2013)

(13) P. Karamanakos, T. Geyer, and S. Manias: "Direct Voltage Control of DC–DC Boost Converters Using Enumeration–Based Model Predictive Control", *IEEE Trans. Pow. Electron.*, Vol.29, No.2, pp.968–978 (2014)

(14) F.M. Oettmeier, J. Neely, S. Pekarek, R. DeCarlo, and K. Uthaichana: "MPC of Switching in a Boost Converter Using a Hybrid State Model With a Sliding Mode Observer", in *IEEE Trans. Industr. Electron.*, Vol.56, No.9, pp.3453–3466 (2009)

(15) D. Takei, H. Fujimoto, and Y. Hori: "Load Current Feedforward Control of Boost Converter for Downsizing Output Filter Capacitor", Proc. of 40th Annual Conference of IEEE Industrial Electronics Society, pp.1581–1586 (2014)

(16) A. Mushi, T. Nozaki, and A. Kawamura: "Proposal for Faster Disturbance Rejection of Boost DC-DC Converter Based on Simplified Current Minor Loop", Proc. of IEEE 2nd International Future Energy Electronics Conference, IFEEC2015, pp.1–6 (2015)

(17) A. Kawamura, T. Haneyoshi, and R.G. Hoft: "Deadbeat Controlled PWM Inverter with Parameter Estimation Using Only Voltage Sensor", *IEEE Trans. Power Electron.*, Vol.PEL–3, No.2, pp.118–125 (1988)

(18) A. Kawamura, R. Chuarayapratip, and T. Haneyoshi: "Deadbeat Controlled PWM Inverter with Modified Pulse Patterns", in *IEEE Trans. Ind. Electron.*, Vol.IE–35, No.2, pp.295–300 (1988)

Appendix

1. Derivation of Sampled Data Nonlinear Model for Boost Converter [8][17][18]

With reference to Fig. 1 whenever the switch is on or off, the converter goes into either of two discrete states (ON or OFF), whose state space equations are:

$$\begin{cases} \dot{x}_i(t) = A_i x(t) + B_i u(t),\ \{i = 1, 2, 3\}, \\ \text{Switch ON, } i = 1,\ kT_s \le\ t < kT_s + \dfrac{\Delta T_1[k]}{2}, \\ \text{Switch OFF, } i = 2, \\ kT_s + \dfrac{\Delta T_1[k]}{2} \le t < kT_s + \dfrac{\Delta T_1[k]}{2} + \Delta T_2[k], \\ \text{Switch ON, } i = 3, \\ kT_s + \dfrac{\Delta T_1[k]}{2} + \Delta T_2[k] \le t < (k+1)T_s. \end{cases} \quad \cdots\cdots \text{(A1)}$$

Note $A_1 = A_3$, $B_1 = B_2 = B_3 = B$, $u(t) = [E\ i_d(t)]^T$. Euler's forward approximation method gives the following discrete time nonlinear model.

$$\begin{cases} x[k+1] = (I + A_1 T_s + A_2 \Delta T_2[k])\, x[k] + BU[k]T_s, \\ A_1 = \begin{bmatrix} -\frac{r_L}{L} & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix}, A_2 = \begin{bmatrix} -\frac{r_L}{L} & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \\ B = \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & -\frac{1}{C} \end{bmatrix}, x[k] = \begin{bmatrix} i_L[k] \\ v_O[k] \end{bmatrix}, U[k] = \begin{bmatrix} E \\ i_d[k] \end{bmatrix} \end{cases} \quad \cdots\cdots \text{(A2)}$$

2. Continuous Time State Space Average Model of Boost Converter

State space averaging is applied to the equation (A1) by integrating and dividing by sampling period T_s gives the following state space averaged model.

$$\begin{cases} \dot{x}(t) = A(t)x(t) + Bu(t) \\ A(t) = \begin{bmatrix} -\frac{r_L}{L} & -\frac{1}{L}\frac{\Delta T_2(t)}{T_s} \\ \frac{1}{C}\frac{\Delta T_2(t)}{T_s} & -\frac{1}{RC} \end{bmatrix} \end{cases} \quad \cdots\cdots \text{(A3)}$$

Note that above, $kT_s = 0$ and discrete time index k was replaced by continuous time index t. Frequency domain model is derived from (A3) and given as (A4)–(A5).

$$v_O(s) = \frac{R}{sRC+1}\left(\frac{\Delta T_2(s)}{T_s} i_L(s) - i_d(s)\right) \cdots\cdots\cdots (A4)$$

$$i_L(s) = \frac{1}{sL+r_L}\left(-\frac{\Delta T_2(s)}{T_s} v_O(s) + E\right) \cdots\cdots\cdots\cdots (A5)$$

3. Tustin Transformation of (10), (11) and (12)

Tustin transformation is given as following.

$$s \text{ is replaced with } \frac{2}{T_s}\frac{z-1}{z+1} \cdots\cdots\cdots\cdots\cdots\cdots (A6)$$

It is used to discretize (10), (11) and (12). The discretized estimated disturbance in (11) is

$$\begin{cases} \hat{i}_d[k] = \left(\dfrac{2-w_{obs}T_s}{2+w_{obs}T_s}\right)\hat{i}_d[k-1] \\ \qquad + \left(\dfrac{w_{obs}T_s}{2+w_{obs}T_s}\right)(i_d[k-1] + i_d[k]), \\ i_d[k] = -i_d[k-1] + \left(\dfrac{\Delta T_2[k-1]}{T_s}\right) i_L[k-1] \\ \qquad + \left(\dfrac{\Delta T_2[k]}{T_s}\right) i_L[k] - \left(\dfrac{2R_nC_n+T_s}{R_nT_s}\right) v_O[k] \\ \qquad + \left(\dfrac{2R_nC_n-T_s}{R_nT_s}\right) v_O[k-1]. \end{cases} \cdots\cdots\cdots\cdots\cdots\cdots (A7)$$

The discretized estimated output current in (12) is

$$\begin{cases} \hat{i}_A[k] = \left(\dfrac{2-w_OT_s}{2+w_OT_s}\right)\hat{i}_A[k-1] \\ \qquad + \left(\dfrac{w_OT_s}{2+w_OT_s}\right)(i_A[k-1] + i_A[k]) \\ \qquad - \left(\left(\dfrac{2-w_OT_s}{2+w_OT_s}\right)\hat{i}_d[k-1]\right) + \hat{i}_d[k], \\ i_A[k] = -i_A[k-1] - \left(\dfrac{2R_nC_n-T_s}{R_nT_s}\right) v_O[k-1] \\ \qquad + \left(\dfrac{2R_nC_n+T_s}{R_nT_s}\right) v_O[k]. \end{cases} \cdots\cdots (A8)$$

The discretized estimated inductance current in (10) is

$$\begin{cases} I_{Lave}[k] = \left(\dfrac{2-w_CT_s}{2+w_CT_s}\right) I_{Lave}[k-1] \\ \qquad + \left(\dfrac{w_CT_s^2}{2+w_CT_s}\right)\left(\dfrac{\hat{i}_A[k-1]}{\Delta T_2[k-1]} + \dfrac{\hat{i}_A[k]}{\Delta T_2[k]}\right). \end{cases} \cdots\cdots\cdots\cdots\cdots\cdots (A9)$$

4. Discussion of Transient Oscillations Observed in Figs. 4 and 5

When (21) is derived, authors assumed that the current $i_L[k]$ is constant, however the transient phenomena in Figs. 4 and 5 it is more reasonable that $i_L[k]$ changes around the $I_{Lave\infty}$ defined in (16) as observed in Figs. 6 and 7. Thus following equation is assumed

$$i_L[k] = I_{Lave\infty} + \Delta i_L[k], \cdots\cdots\cdots\cdots\cdots\cdots (A10)$$

where $\Delta i_L[k]$ is current variation. Using this and taking the same procedures to derive (21) in Section 4.2 yields the next equation

$$\Delta v_O[k+1] = \left(1 - \frac{T_s}{RC}(2+\alpha)\right)\Delta v_O[k], \cdots\cdots\cdots (A11)$$

$$\text{where } \alpha \equiv \frac{\Delta i_L[k]}{I_{Lave\infty}}. \cdots\cdots\cdots\cdots\cdots\cdots\cdots (A12)$$

This equation implies that if α is very large (A11) may oscillate in the transient.

Also it is observed that the large $I_{ref}[k+1]$ causes the duty ratio to be saturated at the upper and lower limits.

In simulation and experiment, it was observed that a very large gain A in (4) made the feedback system unstable. The precise investigation of this nonlinear phenomena is very complicated thus authors believe that this issue is beyond the scope of this paper, thus will be presented later.

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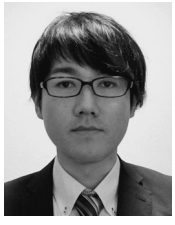

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