SOME METHODOLOGIES FOR FACTS CONTROLLERS

Bakari M. M. Mwinyiwiwa
B.Sc. (Eng) University of Dar es Salaam, Tanzania,
M.Eng. McGill University, Canada

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Department of Electrical Engineering
McGill University
Montreal, Quebec, Canada

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ABSTRACT

Flexible AC Transmission Systems (FACTS) have been conceived to increase the transmissibility of electric power without the necessity of building new transmission lines. An important family of controllers proposed for FACTS are based on high power solid-state switches, such as the gate-turn-off thyristor (GTO), which is presently rated at 6kV, 6kA. The FACTS controller operates at the transmission voltage, in the order of 500kV, and it must be rated at hundreds of MVA. The research of this thesis contributes in developing the methodologies necessary for the integration of the solid-state switches so that the FACTS controllers have the voltage withstand and the current carrying capacity.

The methodologies followed in the thesis are based on organizing the solid-state switches firstly in the forms of: (a) 2-level, voltage-source converter modules or (b) multi-level, voltage-source, converter modules. Thereafter, the modules are connected in series and/or in parallel. Switching strategies such as: (i) the phase-shifted triangle carrier technique and (ii) the fundamental frequency switching, are shown to be promising.

The thesis addresses the methodologies of uniting the modules: (i) in parallel, (ii) in series and (iii) in parallel groups of series-connected modules. Series connections require magnetic transformers. Transformers also enable 6-phase and 12-phase ac systems to be produced from the standard 3-phase ac utility supply. The thesis has initiated research in incorporating the multi-phase ac systems to the multi-modular, multi-level converters.

The thesis has also developed the interface methodology for digital (digital signal processor, DSP) control of the array of modules in real-time.

The methodologies of the thesis have been proven in digital simulations and experimentally in laboratory models.

RÉSUMÉ

Les systèmes flexibles de transport à courant alternatif (FACTS, de l'anglais) ont été conçus dans le but d'accroître les transits de puissance sans pour autant augmenter le nombre de lignes dans un réseau de transport. Une importante famille de contrôleurs proposés pour les FACTS est basée sur des interrupteurs électroniques de haute puissance, comme par exemple les transistors GTO exploités à 6kV et 6kA. Le contrôleur FACTS sera soumis à la pleine tension du réseau, typiquement de l'ordre de 500kV, et devra transiter des puissances de plusieurs centaines de MVA. La recherche décrite dans cette thèse contribue au développment de méthodologies pour intégrer les interrupteurs électroniques dans un contrôleur FACTS pouvant supporter ces tensions et courants de réseau.

Les méthodologies mises de l'avant dans cette thèse explorent deux types de convertisseur: (a) modules convertisseurs à tensions commandées à deux niveaux, et (b) modules convertisseurs à tensions commandées multi-niveaux. Afin d'atteindre les performances requises, les modules sont branchés en série ou en parallèle. Les stratégies d'interruption utilisées sont comme suit: (i) la technique de la porteuse triangulaire déphasée, et (ii) l'interruption à la fréquence fondamentale. Ce deux techniques s'avèrent prometteuses.

Cette thèse fait l'étude des branchements des modules élémentaires (i) en parallèle, (ii) en série, et (iii) en groupements séries branchés en parallèle. Les branchements séries font appel à des transformateurs magnétiques. La présence de ces transformateurs permet également de produire des convertisseurs à 6 ou à 12 impulsions à partir de l'alimentation triphasée. Nous abordons égalment le branchment de convertisseurs aux configurations multi-modulaires et multi-niveaux à des réseaux d'alimentation multiphasés.

La thèse présente également une méthodologie pour implanter la commande numérique du contrôleur en temps réel.

Des simulations numériques et des essais sur prototype en laboratoire ont permis de valider les méthodologies proposées dans cette thèse.

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LIST OF MAIN SYMBOLS

C	Capacitor
f_c	Carrier frequency
f_m	Modulating frequency
φ_{REF}	Reference angle
I	Current
I_{dc}	Dc current
K_c	Number of triangles per modulating cycle
L_f	Filter inductance
R_f	Resistance of filter inductance
T_c	Period of carrier signal
T_m	Period of modulation signal
T_s	Sampling period
V, v	Voltage
V_{tc}	Triangle carrier signal
V_m	Modulation signal
V_{dc}	Dc voltage
V_{REF}	Reference voltage
X_f	Filter reactance
X_L	Line reactance

LIST OF ACRONYMS

AC, ac	Alternating Current
A/D	Analog to Digital
BJT	Bipolar Junction Transistor
COM PORT	Communication Port
CSI	Current Source Inverter
D/A	Digital to Analog
DC, dc	Direct Current
DSP	Digital Signal Processor
FACTS	Flexible AC Transmission System
FBI	Full-Bridge Inverter
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Array
GDB	Gate Drive Board
GTO	Gate Turn-Off Thyristor
HVDC	High Voltage Direct Current
IEEE	Institute of Electrical and Electronic Engineers
IGBT	Insulated Gate Bipolar Transistor
LDG	Logic Design Group
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MCT	MOS-Controlled Thyristor
M.I.	Modulation Index
MVA	Mega Volt Ampere
MVAR	Mega Volt Ampere Reactive
NPC	Neutral Point Clamped
PC	Personal Computer
PCB	Printed Circuit Board
PI	Proportional plus Integral
PLD	Programmable Logic Device

PLL	Phase Lock Loop
PWM	Pulse Width Modulation
RAM	Random Access Memory
RMS	Root Mean Square
SIT	Static Induction Transistor
SITH	Static Induction Thyristor
SPWM	Sinusoidal Pulse Width Modulation
SCR	Silicon Controlled Rectifier
STATCOM	Static Compensator
SVC	Static VAR Compensator
SVG	Static VAR Generator
THD	Total Harmonic Distortion
UPFC	Unified Power Flow Controller
VAR	Voltage Ampere Reactive
VCO	Voltage Controlled Oscillator
VSI	Voltage Source Inverter

CHAPTER I

INTRODUCTION

1.1 Historical Perspective of Power Electronics

Power Electronics began with the vacuum tube diode which made ac to dc rectification possible [1]. The advent of the thyratron [1], with the gate-turn-on capability, introduced an element of controllability. By delaying the gating pulse, it became possible to control the amount of rectified power [2]. The turn-off of the thyratron depended on the negative half of the ac voltage cycle or what is called, line-commutation. A whole technology has developed around the line commutation concept: the Graetz bridge [2], the line-commutated inverters [3], the High Voltage Direct Current (HVDC) Transmission System [2], the Static VAR Controller (SVC) [4,5], the cycloconverters [3].

By the mid-1960s, the solid-state thyristors, i.e., the Silicon Controlled Rectifier (SCR) [6] replaced the thyratrons and the mercury-arc rectifiers [1] in the line-commutated technology. Like the thyratrons, the thyristors have gate turn-on capability but have to be turned OFF by the reversal of the anode-cathode voltage. Apart from line-commutation, this voltage reversal can also be achieved by a force-commutation circuit which turns ON an auxiliary thyristor to connect the reversed voltage from a previously charged capacitor to the principal thyristor [7,8]. The force-commutated thyristors enable dc-to-ac inversion to be carried out over a range of operating frequencies for variable speed ac motor drives [9,10].

As the research in the variable speed ac motor drives progressed , it became clear that the ac voltage amplitude must be coordinated with the motor speed [11]. When the

inverter source is a fixed dc voltage or dc current, the amplitude control can be achieved only by Pulse Width Modulation (PWM) [12], that is by controlling the relative durations of the ON and the OFF states of the force-commutated thyristors.

Originally the force-commutated thyristor circuits were slow, complex and costly. In the past two decades, the solid-state industries have produced a range of power switches which have both gate-turn-on and gate-turn-off capabilities [13]. These switches are given the general name "valves" in this thesis. Fig. 1.1 shows a schematic and symbol of a generic "valve". Some of these valves are Bipolar Power Transistors (BJTs) [14], power Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) [15], Insulated Gate Bipolar Transistors (IGBTs) [16], Static Induction Transistors (SITs) [14]. They cover a broad ranges of switching speeds, voltage and current ratings. Tending to be slower but reaching to the higher voltage and current ratings are the Gate-Turn-Off thyristors (GTOs) [17], the Static Induction Thyristors (SITHs) [18] and MOS-Controlled Thyristors (MCTs) [19]. The symbol for the "valve" shown in Fig. 1.1(b) will be used throughout in this thesis to represent a power electronic (solid-state) switch with gate-turn-on and gate-turn-off capability. The "valve" may be a single power electronic (solid-state) switch or a series and/or parallel combination of several switches which receive a common gate control signal for turning ON or OFF.

The availability of these valves has given a great impetus to the development of different methods of static power processing. For low and medium power

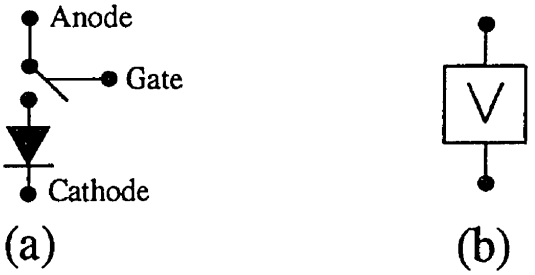


Fig. 1.1: Power Electronic valve.
(a) Functional schematic. (b) Symbol.

applications such as ac motor drives, different methods of pulse width modulation (PWM) have been developed. In addition to controlling the frequency and the amplitude of the fundamental frequency of the modulating signal, the objectives have been broadened to include the control of the harmonics so as to reduce the motor torque pulsations [11,20,21]. As a result, there is abundant literature on PWM methods [22,23].

The success in low and medium power applications has led to the challenge of extending power electronics to the electric utility environment. Recognizing that the GTOs by then were beginning to be available in the 3kV and 1kA range, the Electric Power Research Institute (EPRI) of USA fostered Research and Development (R&D) on Flexible AC Transmission Systems (FACTS) [24] based on high power electronic controllers.

The objective of the FACTS initiatives of EPRI is to increase the transmissibility of power through the existing network by the installation of fast FACTS controllers so that no new transmission lines need to be built. The FACTS controllers provide voltage support as in the shunt-STATCOM [25,26], compensate the inductive line reactance as in the series-STATCOM [27] or they combine phase-shifting and VAR compensation as in the Unified Power Flow Controller (UPFC) [28]. By the fast action of the power electronic switching, the FACTS controllers increase the transient stability limit beyond the levels which are presently set by the slow field excitation systems of the alternators, the power system stabilizers and the transformer tap-changers [26,29,30].

For high power applications, however, the voltage and current ratings of the individual power electronic switches are still far below the requirements of the electric power utility. As a consequence, different methods of achieving high power requirements from the available solid-state switches have been proposed. These are: series and parallel

connection of individual switches [31-34], series and parallel connection of 2-level converters [31,32,35-37] and multilevel converters [38-44]. In general, high power valves are slow and the switching rates have to be kept at the lowest possible levels in order to minimize switching losses. Low switching rate has the following drawbacks: (1) limited frequency bandwidth resulting in slow response, (2) low order harmonic content in the output voltage which will need expensive harmonic filters.

This thesis consists of research on the synthesis of static power converters for high power applications. The basic building blocks of the synthesis are: (1) 3-phase, 2-level voltage source converter of Fig. 1.2, and (2) the 3-phase, diode-clamped multilevel converter of Fig. 1.3. To date, the technologies for these two converter topologies have already a modest literature [35,37,41,42]. The study presented in this thesis will concentrate on the different methods of combining the basic building blocks to achieve high voltage and high current ratings, low harmonic content and current equalization among the individual valves.

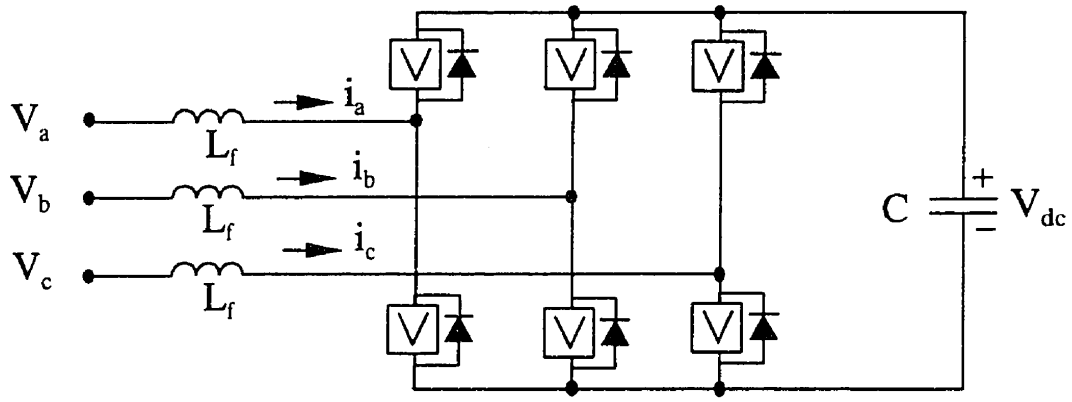


Fig. 1.2: Schematic of a 3-phase 2-level voltage source converter.

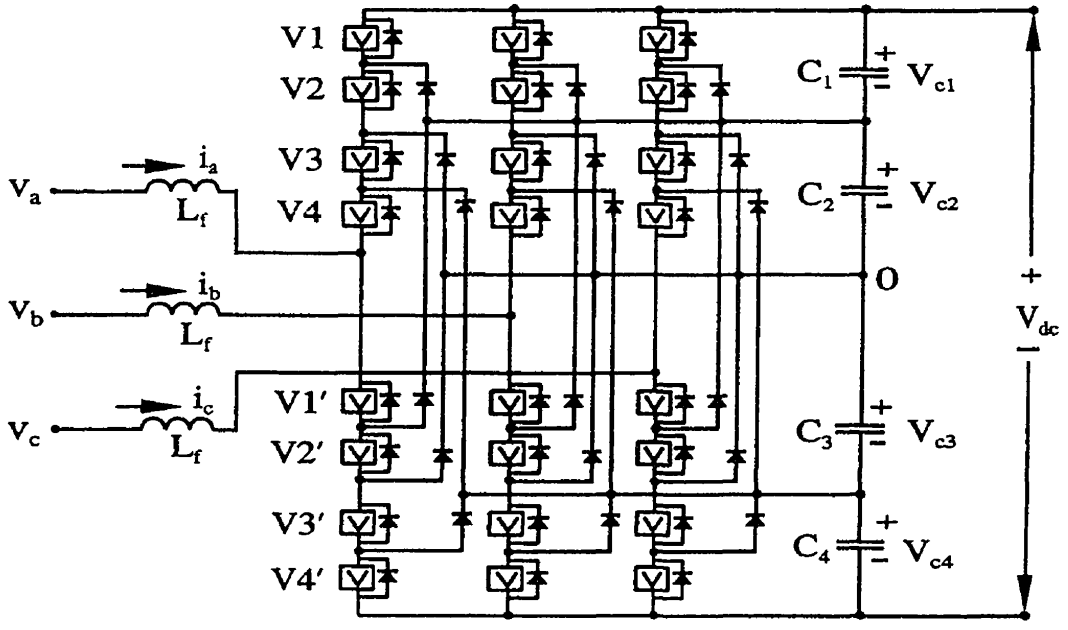


Fig. 1.3: Schematic of a 3-phase 5-level diode-clamped converter.

The thesis work contains simulations as well as experimental work. Digital simulations are relatively easy to implement as it is a matter of writing software to describe the circuit equations of a given topology. On the other hand, experimental verification requires the building of hardware. In the laboratory, 6 modules of 3-phase 2-level voltage source converter of Fig. 1.2 have been built and they form the building blocks of the experimental research on multiple modules of Fig. 1.2 and multilevel converters. A few words of explanation are needed to justify the many experimental research on multilevel converters that has been carried out.

For practical reasons related to bracketing the valves safely within the dc capacitor voltages, the diode-clamped topology of Fig. 1.3 is the circuit which will be used in the field. For this reason, the research contains extensive digital simulations of the 5-level,

diode-clamped circuit. The 5-level and all odd-levels cannot be represented by modules of Fig. 1.2 without additional diodes. For this reason, all experimental studies on the multilevel converters are based on even number of levels: 6-level and 4-level.

In the experimental tests which involve multilevel converters, five modules of 3-phase 6-valve converters of Fig. 1.2, have been used to configure a 6-level converter shown in Fig. 1.4. And a 3-phase 4-level converter shown in Fig. 1.5 has been configured using three modules of Fig. 1.2. It has to be stated here that, the multilevel topologies used in the laboratory experimental tests (Fig. 1.4 and 1.5) are not suitable for high power applications due to unequal voltage distribution across the valves. These laboratory models of the 6-level and the 4-level converters were used to obtain experimental verification of the theoretical and/or simulation findings.

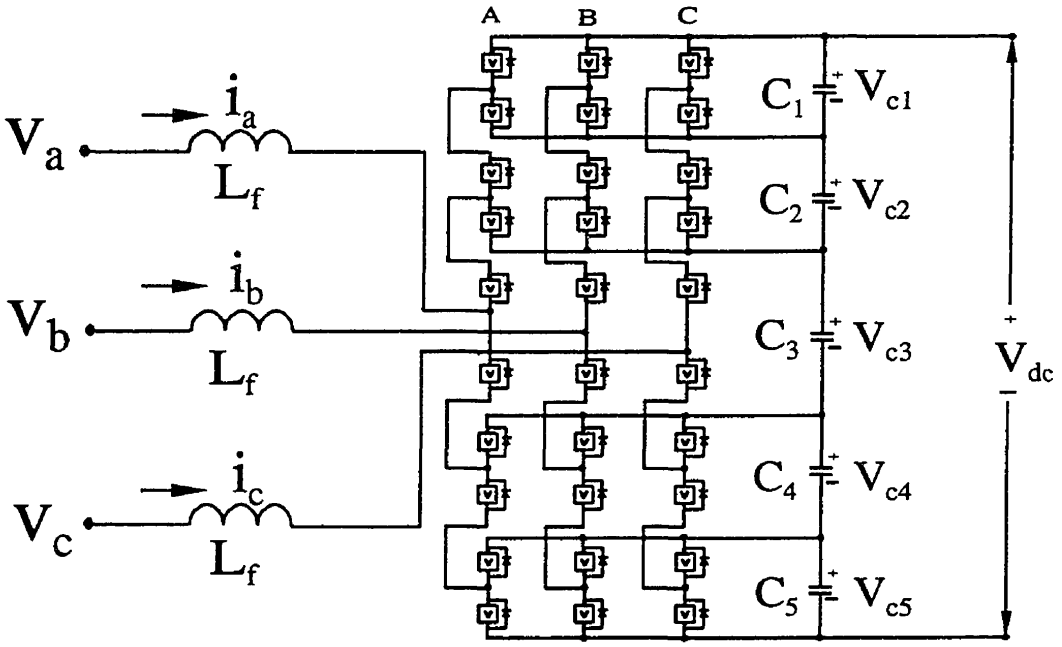


Fig. 1.4: Schematic of laboratory 6-level converter.

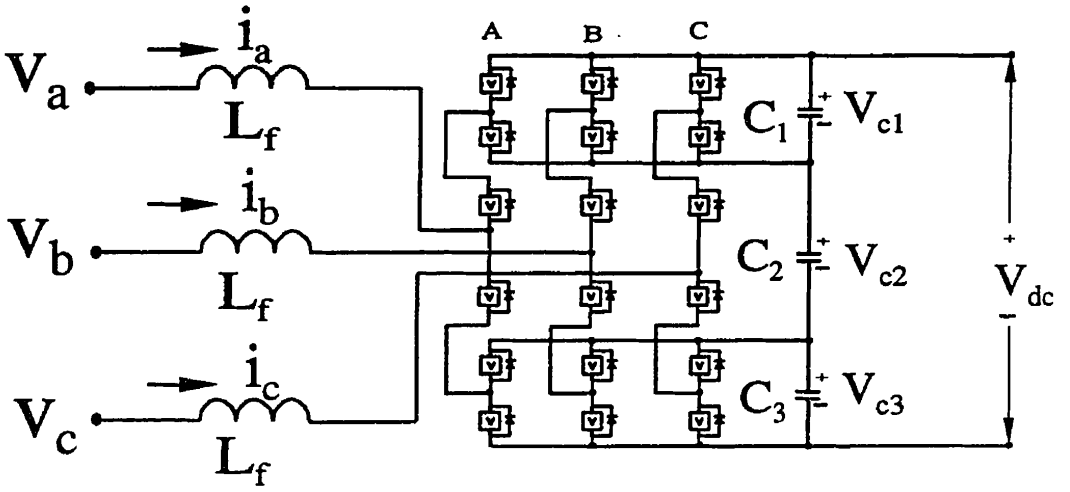


Fig. 1.5: Schematic of laboratory 4-level converter.

1.2 Review of Previous Work on Electronic Power Processing for High Power Applications

The difference between the power electronics converters designed for high power applications and the ones intended for low or medium power applications goes beyond the simple scale factor. The main reason is that, while the high power converters have to operate at hundreds of kV and several kA, where as the ratings of the high power solid-state switches available today, as exemplified by the GTOs, are limited to 6kV and 6kA only [45]. Furthermore, the highest switching rate ever applied to the GTOs is 540Hz [37].

The methods of augmenting the voltage and/or current ratings ultimately consists of connecting the solid-state switches in series and/or in parallel. However, the schemes fall into 3 general classifications:

(1) Multi-device: series and/or parallel connections of the solid-state switches to

form valves.

(2) Multiconverters: series and/or parallel connections of the solid-state switches or valves which are already in the forms of bridge modules such as in Fig. 1.2.

(3) Multilevels: series connection of the solid-state switches or valves organized as multiple levels as in Fig. 1.3, for example.

1.2.1 Multi-device

The common practice used to increase the voltage withstand is to use valves, which are composed of several single solid-state switches connected in series. Similarly, the current rating can be increased by having valves composed of several individual solid-state switches connected in parallel. As a result, the high MVA rating can be achieved by employing valves which are composed of series and parallel connected solid-state switches. This technique has been used since the era of thyratron up to the present, for synthesizing high power electronic power processors such as line-commutated HVDC transmission systems [31,32,37,46], GTO based Static VAR Compensators [25] and GTO based Static VAR Generators [26,29,47]. The main problem of combining individual power electronic switches in series and/or parallel is that some auxiliary passive circuits have to be employed so as to ensure the equalization of voltages and currents. This is because it is not possible for the manufacturers to provide all the power electronics switches with exact switching characteristics. The losses in the passive circuits lower the efficiency. To ensure voltage and current equalization, solid-state switches must switch ON and OFF simultaneously.

The valves which are composed of several single solid-state switches connected

in series and parallel, form high power switches to build high power static power converters [29,37]. There are mainly two categories of static power converters. They are the voltage source converter shown in Fig. 1.2 [37,48-50] and the current source converter which is depicted in Fig. 1.6 [51-53].

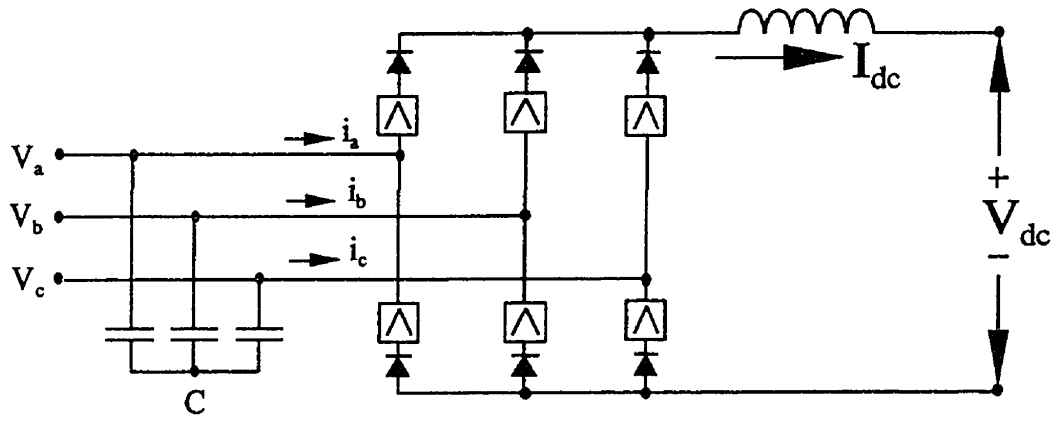


Fig. 1.6: 3-phase current source converter.

1.2.2 Multiconverters

The converter modules of Fig. 1.2 and Fig. 1.6 are conceived as the building blocks for the realization of high power converters for use in Flexible AC Transmissions Systems (FACTS) such as HVDC Transmission systems [35,37,46], STATCOMs [25,26] and UPFC [28]. This method is already in application, as in most of the early line-commutated HVDC Transmission systems [31,32], four 3-phase 6-pulse current source converters of Fig. 1.6 are connected in series on the dc side. On the ac side, four sets of 3-phase transformers are used, two sets connected in wye-wye and the remaining two sets connected in wye-delta. This arrangement has the advantage that the sixth harmonic on the dc link is eliminated leaving the residual 12^{th} harmonic, hence the name

12-pulse converter was given [31,32]. The 5^{th} and the 7^{th} harmonics are eliminated in the ac waveform. Another advantage of the 12-pulse converter is that in case of failure of one converter, the remaining converter can continue to deliver power to the load.

In the STATCOMs installed in USA and Japan [25,26], GTOs have been used as basic solid-state switches so that turn-off is achieved by gate signals. Both STATCOMs use 8 modules of 3-phase 6-pulse GTO voltage source converters of Fig. 1.2. The converters are switched at power system frequency. According to [26], the switchings of the 8 converters are equally staggered in time so that the output voltages of the modules are not in phase. Then a special transformer arrangement is used to synthesize them into a staircase equivalent voltage waveform. The synthesized staircase voltage is then stepped up to the transmission voltage level using another transformer stage. The GTOs switch at a rate of 1 pulse per 60Hz cycle so that the switching loss is minimum.

In an on-going research in Japan [37], there is an early attempt to use Pulse Width Modulation (PWM) in high power application. Though it has not been expressly stated, from the description in [37], one can clearly conclude that "phase shifted triangle carrier" technique [36] to operate the converters has been used. In their prototype, they use 4 modules of 3-phase, 6-pulse voltage source GTO converters (Fig. 1.2) which are connected in series by transformers. The switching frequency for each converter is 500Hz, and as a result the equivalent switching rate for the 4 modules is 2000Hz.

1.2.3 Multilevel

Another approach of increasing the MVA ratings is the use of the multilevel concept [38-44]. The multilevel topology has three main advantages. First, the high

voltage withstand is obtained by the series summation of the voltages across the dc capacitors. By feedback regulation of the dc capacitor voltages so that they are safely below the ratings, the solid-state switches which are connected across them are protected against overvoltages. The solid-state switches connected between the dc buses of the different levels of the dc capacitors do not have to switch simultaneously. Thus the necessity of achieving simultaneous switching is bypassed. Secondly, in the medium voltage range, such as 13kV distribution system, multilevel converters may be connected directly, in applications such as STATCOMs [40,42,44,55], without the necessity of the coupling transformer and this means saving in cost. The third advantage is that, in the case of fundamental switching, selected harmonics can be eliminated by choosing switching angles [44,54,55]. This feature makes multilevel converters attractive in medium power applications such as in ac motor drives [55,56].

Historically, the multilevel converter topology began with Nabae's invention [31] of the "Neutral Point Clamped" (NPC) converter. Since then, several research groups developed on Nabae's idea [39-44,54-64]. Presently, there are three known topologies of multilevel converters. The first topology is the diode-clamped which has been based on the NPC configuration [38]. Fig. 1.3 is an example of NPC converter [40,64]. In the diode-clamped multilevel converter, the same dc capacitors are connected to all the 3-phase converter legs.

Another topology termed "flying capacitor" multilevel converter is shown in Fig. 1.7 [40,64]. In this topology, the dc capacitors are of different voltage ratings. Separate capacitors are used for each phase of the multilevel converter.

In 1995, a new topology of multilevel converter with the name "multilevel

cascade" was introduced [63,64]. In this topology, each phase leg of the inverter is composed of (M-1)/2 Full Bridge Inverter (FBI) units connected in cascade to form an M-level output voltage. Fig. 1.8 shows an example of a 3-phase 5-level cascade inverter. Each full-bridge inverter has its own regulated dc voltage source derived from its dc capacitor.

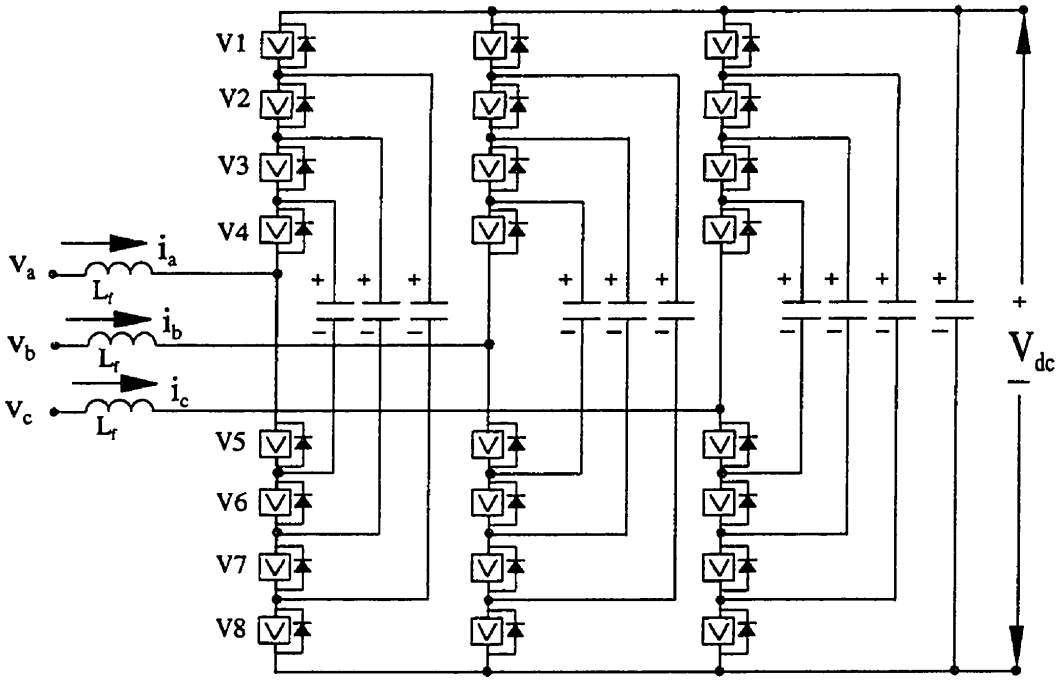


Fig. 1.7: 3-phase 5-level flying capacitor converter.

1.3 Objectives and Scope

The objectives of this thesis are to study the methodologies for attaining high voltage and high current rating for FACTS controllers. The constraints which have to be met are: (1) the switching losses of the solid-state switches must be minimum, (2) the voltage stresses and the current loadings of the solid-state switches must be shared

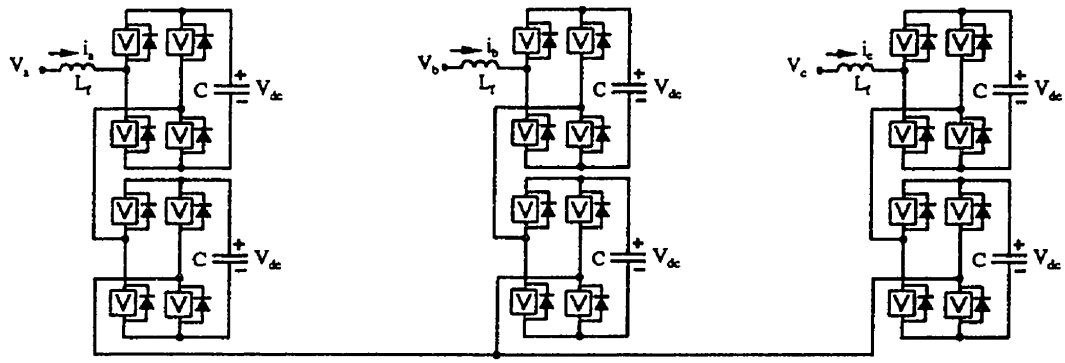


Fig. 1.8: Wye connected 3-phase 5-level cascade converter.

equally, (3) the Total Harmonic Distortion (THD) factors of voltages and current waveforms must meet the harmonic standards.

The scope of the thesis is restricted by the four-year period allowed by the University of Dar es Salaam in granting the study leave. The allotted time has been used in examining (1) the multiconverter (Part 1, chapters II and III) approach and (2) the diode-clamped multilevel converter (Part 2, chapters IV through VI) approach.

1.4 Methodologies of the Thesis

As the theoretical foundations of the area of research are not developed, the mainstay of the research methods are digital simulations and experiments.

The simulation studies on the high power FACTS controllers have been done by writing programs in the C-language and MATLAB software [65]. Whenever possible, the simulation results were verified on the experimental facility. The successful simulation runs were used as indicators to go ahead to the experimental tests. Sometimes the algorithms used in the simulations were ported (with only few modifications) into

programs which were compiled to run in the Digital Signal Processors (DSPs) of the controllers of the experimental facility. In the case of fundamental switching technique, simulation programs were used to generate the switching patterns used by DSPs to control the experimental converter.

In order to perform experimental based studies, it was necessary to design, construct and commission a laboratory size research facility. At the outset, it was decided the facility should have the flexibility and versatility for programs of experimental research on multiconverters and multilevel converters. Presently, the experimental facility consists of six modules of 2-level 3-phase voltage source converters (Fig. 1.2), each rated 5kVA. Each module is made of standard commercially available half-bridge IGBT power modules rated at 600V, 50A per device. IGBTs are voltage controlled devices and as such they need very low gate drive power and simple gate drive circuitry.

Some of the power electronic circuits which have been configured for the tests reported in the thesis using the available facility are: the 2-level multiconverters (Fig. 1.2), the 6-level converter (Fig. 1.4) and the 4-level converter (Fig. 1.5). For the purpose of enhancing flexibility, a digital control facility has been developed by Prof. Z. Wolanski which incorporate Field Programmable Gate Array (FPGA) devices. Prior to FPGA, the auxiliary circuits had been analog circuits which had to be corrected for drifts. The FPGA devices also enable the user of the facility to reconfigure the layout and the circuit topology very quickly within a few hours. In order to reduce the bulk of the thesis, the details of the experimental facility are not included. The outlines of building blocks of the experimental facility are summarised in the appendices. More details have been compiled in a separate laboratory manual [66].

1.5 Contributions

In the candidate's best knowledge (and this belief is supported by the referees who accepted the transactions or conference publications), the following are original contributions in the two approaches:

PART 1: MULTICONVERTER APPROACH

(1) The relative merits of series and parallel connections of the multi-modules using magnetic transformers (chapters II and III).

(2) Methods of current equalization in multi-module connections of 2-level voltage source converters operated by the lowest rate of $f_c / f_m = 3$ of the phase-shifted triangle carrier technique of the Sinusoidal Pulse Width Modulation (SPWM) strategy (Chapter II). The major conclusions are (section 2.5): (i) For 3 pulses, 2-level converters, 2 modules in series connection will equalize the currents for Modulation Index (M.I.) of less than 0.8, and slight current unbalance for M.I. greater than 0.8. (ii) For 3 pulses, 2-level converters, 4 modules in series connection will equalize the currents for the full range of M.I.

(3) The 7-Timer Method described in chapter III (section 3.6) which enables 2-level multiconverters to be operated digitally using the phase-shifted triangle carrier technique of the Sinusoidal Pulse Width Modulation (SPWM) strategy. The 7-Timer Method in its final form is an algorithm executed by the Digital Signal Processors (DSPs), which through the FPGA interface, channels the ON-OFF logic commands to gate the drives of the IGBT switches of the multiconverters. The technique has been tested successfully in simulations and experimentally using

four and six 3-phase converter modules. The technique is an extension of the existing 4-Timer Method which is limited to a single 3-phase converter [67,68].

PART 2: MULTILEVEL CONVERTER APPROACH

(4) A significant discovery that it is possible to operate the SPWM strategy at the lowest switching rate of 1 pulse per modulation cycle using multimodules of the multilevel converter (chapter IV and [69]). This is an important step because the 1 pulse per modulation cycle represents minimum switching loss. The phase-shifted triangle carrier SPWM strategy enables signals of a broad frequency bandwidth to be transmitted. The multiple modules of multilevel converters represent very large power amplification.

(5) Concept and realization by laboratory experimental demonstration of a series-STATCOM based on the multilevel topology. The tests the series-STATCOM had been subjected to were: (a) steady-state balanced operation, (b) unbalance faulted conditions.

(6) Improvement of the performance of the multilevel converter station by first transforming the 3-phase ac power supply to a 6-phase or a 12-phase ac sources which then feed 2 or 4 modules of multilevel converters. The modules are connected in parallel to the dc link capacitors of the different levels. The improvements come in: (1) the reduction of the ripples in the dc voltage waveform at all levels and (2) the lowering of the cost as the size of the dc capacitors can also be reduced.

1.6 Organization of the Thesis

This section provides an overview which shows that they form a coherent research effort. The goal of the research is to develop the methodologies to increase the voltage and MVA ratings of the controllers of the Flexible AC Transmission Systems (FACTS). The research seeks to reach the hundreds of kVs and MVAs requirements of FACTS controllers by solid-state switches which are individually rated at 6kV and 6kA, as in the case of GTOs, by two approaches based on circuit topologies:

Part 1 - the multiconverter approach (chapters II and III)

Part 2 - the multilevel converter approach (chapters IV, V, VI).

Part 1: Multiconverter Approach

Prior to the research of this thesis, McGill University has already made advances in the multiconverter approach, notably in the phase shifted triangle carriers technique of the Sinusoidal Pulse Width Modulation [SPWM] strategy [35,36]. However, the research of [35,36] has been entirely based on digital simulations. The logical next step which is carried out in this thesis, consists of proving the practicability of the strategy in laboratory experimental models. Accordingly, the candidate designed and built a laboratory facility for multiconverter research, which consists of 6 modules of the 3-phase , voltage source bridge converter. The laboratory facility is digitally controlled by a DSP platform (Hydra II DSP mother board from Ariel company which contains four Texas Instruments TMS320-C40 DSPs), in conjunction with two Field Programmable Gate Array (FPGA) devices. The digital controls were designed and built by Prof. Z. Wolanski.

Chapter II: The multiconverter laboratory facility in conjunction with analysis and simulations have been used as a research tool to investigate the practical means of integrating the 2-level, 3-phase voltage source bridge converter modules. Emphasis is placed on the lowest pulse rates which has the lowest switching losses. Unfortunately, the voltages of the individual converter modules are unbalanced so that they cannot be connected in parallel. The balancing methods investigated are: parallel connections, series (with transformers) connections and parallel connections of series (with transformers) groups.

Chapter III: The phase shifted triangle carrier technique of the Sinusoidal PWM strategy has been implemented in off-line digital simulation by comparing the sinusoidal modulating signal and the triangle carriers and using their intersection instants in the integration step to "trigger" the solid-state switches ON or OFF in the simulation program. In the real-time implementation of the experimental facility, it is too costly to commit DSPs to monitor the signals for the intersecting instants. Instead, in Bowes's 4-Timer Method [67,68], the 3 modulating signals of the 3-phase ac are sampled periodically at the period of one timer and based on the samples, the switching times for each of the 3-phases are computed and loaded on the remaining 3 timers. The switches of the 3-phases of the bridge converter are triggered upon the count-down of the 3-timers.

Chapter III extends the 4-Timer Method of one converter module to the 7-Timer Method which is suitable for N converter modules, N being an integer number as long as it is even and within the computation speed of the DSP. The 7-Timer Method is important not only because it requires a small number of timers but also because it

Method which is suitable for N converter modules, N being an integer number as long as it is even and within the computation speed of the DSP. The 7-Timer Method is important not only because it requires a small number of timers but also because it reduces inaccuracies so that the equivalent sampling frequency approaches the theoretical limit of Nf_c set by the shifted triangle carrier technique of the SPWM strategy.

Part 2: Multilevel Converter Approach

As the diode-clamped, multilevel approach published for the first time by A. Nabae [38] holds promising advantages, the second part of the thesis has devoted research to it. The work is described in chapters IV, V and VI.

Chapter IV: Hitherto, only single unit multilevel converters has been studied. This chapter documents the research on multiple modules of the diode-clamped multilevel converters. Multiple modules of multilevel converters are operated under the phase shifted triangle carrier Sinusoidal Pulse Width Modulation (SPWM) strategy in digital simulations.

In the course of the experiments in the digital simulations, an important discovery of practical consequence has been made. The simulation results have shown that using 8 modules of multilevel converters operated with phase shifted carriers, the switching rate for individual valves can be reduced to as low as a single pulse per modulating cycle without serious deterioration in the total harmonic distortion (THDs) in the waveform and in the capability to operate as 3 high-power linear amplifiers with constant gain.

Furthermore, this chapter has initiated research on faults to the steady-state studies.

Experimental results obtained from a laboratory series-STATCOM based on multilevel converter are presented. The test results have shown that multilevel converter operated as series-STATCOM with delta-wye connected coupling transformer is capable of operating as a capacitance even under fault conditions while maintaining the total dc voltage regulation and individual dc capacitor voltage equalization. The test results also have shown that the multilevel series-STATCOM is capable of turning OFF safely which corresponds to virtually inserting the large magnetizing inductance of the coupling transformer into the transmission line. It is also capable of re-inserting itself into the transmission line after the turn OFF.

Chapter VI: One weakness of the diode-clamped, multilevel converter topology is that the dc voltages across the dc capacitors of each of the multilevels contain inherent third and triplen harmonics. The third and triplen harmonics affect adversely the total harmonic distortions (THDs) in the ac voltage and current waveforms, derate the ratings of the solid-state switches and complicate the design of the feedback loops.

In chapter VI, a method of reducing triplen harmonics on the dc capacitor voltages of multilevel converters is described. When a single module of multilevel converter is used as STATCOM for example, the dc capacitor voltages contain large third harmonics. When two multilevel converters are configured as supplied from a 6-phase ac source, the third harmonics on the dc capacitor voltages are eliminated leaving residual sixth harmonics. Simulation results confirmed by experimental test results on a 6-phase, two multilevel converters operated as a shunt-STATCOM are presented. Simulation studies

have shown that the residual sixth harmonics can also be eliminated by using four multilevel converters configured as a 12-phase STATCOM.

Chapter VII gives a summary of the thesis and conclusions. Furthermore, some suggestions are given for future work as a follow up of the research work presented in this thesis.

PART 1:

2-LEVEL 3-PHASE CONVERTERS

CHAPTER II

MULT-MODULES OF 2-LEVEL 3-PHASE CONVERTERS

2.1 Introduction

The GTOs in the 100 MVA and 80 MVA STATCOM installations in U.S.A. and Japan respectively, [25,26] switch at the rate of 1 pulse per 60Hz period, which incurs minimum switching loss. The research of this chapter is aimed at the near future when GTOs can switch at higher frequencies and IGBTs at higher frequencies still, and the Sinusoidal Pulse Width Modulation (SPWM) technique can be applied to FACTS (Flexible AC Transmission System) controllers so that they have the benefits of direct magnitude control and output-to-input linearity for the implementation of sophisticated modern control theory and active filtering. The availability of faster high power solid-state switches will allow the pulse rates to increase firstly to 3 and then to 9 pulses per 60Hz period [37] and higher. The Total Harmonic Distortion (THD) standards can be met at such low switching rates by applying the Phase Shifted Triangle Carrier SPWM technique [35,36,67,70] to control multiple modules of the GTO converters.

This chapter addresses the issue of equalizing the currents in the FACTS stations based on multiple SPWM converter modules. Firstly, it is instructive to review how this is accomplished in the Japanese STATCOM [26], which has a fuller disclosure of the design which is based on 8 parallel, 3-phase voltage source converter bridge modules. The individual modules produce 8 sets of identical 3-phase square voltage waveforms which are phase shifted. A staircase waveform approximating the sinusoid is obtained for each phase, upon summation of the 8 square waveforms. However, because of the phase-shifts

in the voltages, the outputs from the parallel modules cannot be connected directly to a common set of nodes without causing large circulating currents. This is solved by using phase shifting transformers, one set for each module, between the converter modules and the station buses. A second set of transformers then raises the voltages from the low voltage levels of GTOs to the high transmission line voltages.

The Phase Shifted Triangle Carrier SPWM technique has the property that the output contains the modulating signals which are amplified by the same constant gain without phase shifts. Thus in general, the outputs of the multiple modules can be connected directly in parallel so that the phase-shifting transformer stage will not be necessary for pulse rates of 9 and higher. Thus only the step-up voltage transformers are required, saving the cost of the intermagnetic stage. However, in the interim period of waiting for the faster GTOs [46] or the more powerful IGBTs to be available and the 3 pulses per 60Hz period will have to be used, the cost of the first stage is unavoidable. For the case of 3 pulses per 60Hz period, the lower sideband switching noise of the Phase Shifted Triangle Carrier SPWM Technique will have the same frequency as the 60Hz signal. Consequently, the 60Hz voltages of the modules are unbalanced so that they cannot be connected directly to the step-up voltage transformers. Thus an intermagnetic stage based on transformers is also necessary for equalizing the currents from the multiple modules.

2.2 Voltage Source Converter and Sinusoidal Pulse Width Modulation

Fig. 2.1(a) shows the schematic of the 3-phase voltage source converter. Its single line equivalent circuit is shown in Fig. 2.1(b), with the ac terminals 'a' and 'n' denoting

the a-phase and the neutral respectively. Fig. 2.2(a) and (b) illustrate the well known technique of generating ac output from a modulating signal at frequency f_m, and a triangle carrier at frequency f_c. Fig. 2.3 illustrates the typical frequency spectrum of the SPWM waveform (f_c=21f_m) [67,12]. The amplified modulating signal is located at frequency f_m. The switching noise power is contained in the carriers which are located at frequencies f_c, $3f_c$... and the sidebands, at f_c-2f_m, f_c+2f_m, 2f_c-f_m, 2f_c+f_m, 2f_c-3f_m, 2f_c+3f_m, 2f_c-5f_m...

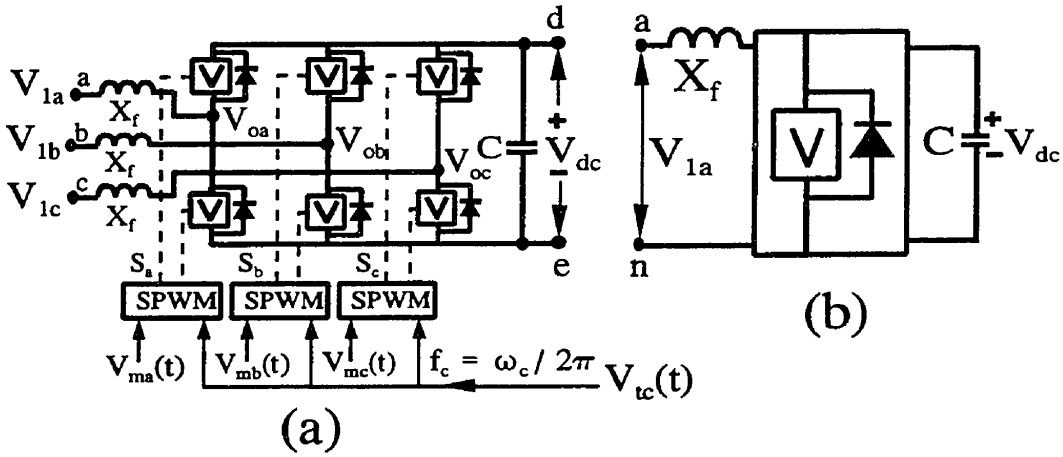


Fig. 2.1: Voltage Source Converter. (a) Schematic diagram. (b) Single line equivalent circuit diagram.

For high power applications, switching loss consideration rules out using GTOs at f_c which is higher than 540 Hz [46]. However by using L_m multimodules as described in the next section, the effective carrier becomes $L_m f_c$. The spectrum of the total output takes the same form as Fig. 2.3 with the modification that the carrier frequency f_c is replaced by $L_m f_c$. Thus the noise components are shifted to the high frequency end where the filtering components are cheaper to realize.

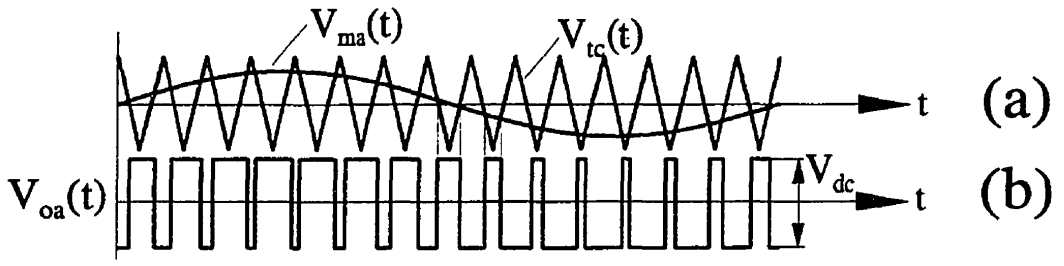


Fig. 2.2: Sinusoidal Pulse Width Modulation. (a) Modulating signal and Triangle carrier. (b) PWM output voltage.

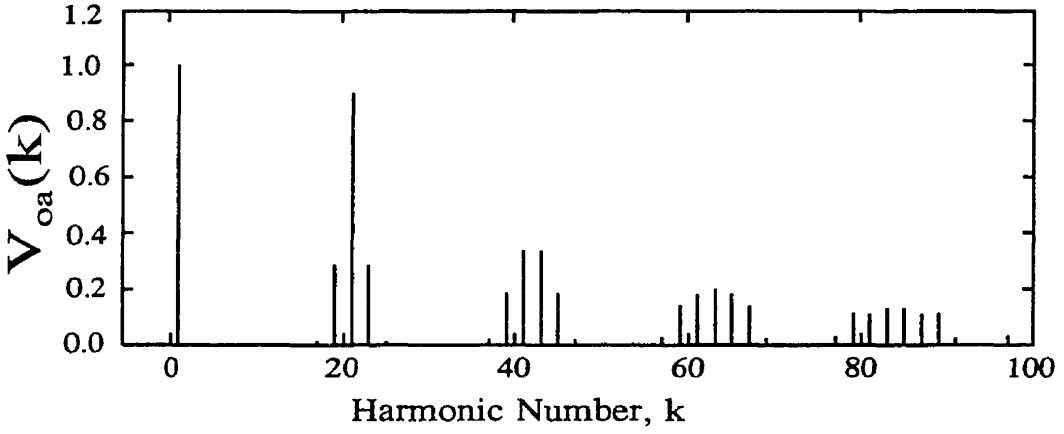


Fig. 2.3: Spectrum of SPWM output voltage, $V_{oa}(t)$.

2.3 Multiconverters with Phase Shifted Triangle Carriers [35,36]

By sending phase shifted triangle carriers as illustrated in Fig. 2.4 to each of the L_m converter modules, the switching instants of the GTOs are staggered as the intersection points of the carriers with the common modulating signal are different for each converter. The summation of the ac outputs from L_m converters yields a high quality output with the

spectrum similar to that of Fig. 2.3, with the important advantage that the effective carrier frequency is increased to $L_m f_c$ without incurring higher switching losses.

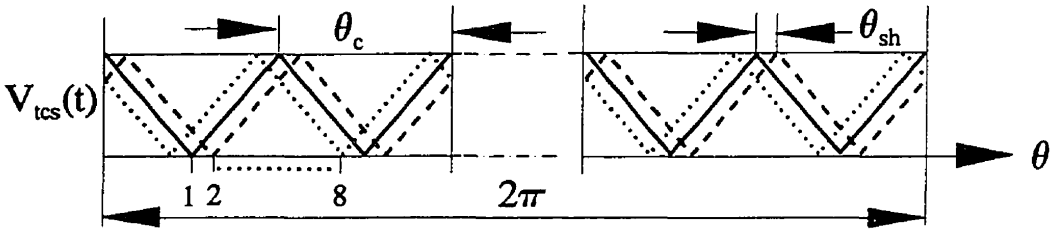


Fig. 2.4: Phase shifted triangle carriers for 8 converter modules (only L_m = 1,2 and 8 are shown).

2.3.1 Choosing Carrier Frequency as Triplen of Modulating Signal

When the 3 ac-phases of each converter module are connected to a balanced delta circuit or to a balanced open wye circuit, the zero sequence currents (which include the triplen harmonics) cannot flow. When the circuit has this inherent triplen discrimination, it is advantageous to choose the triangle carrier frequency to be an integral multiple of 3 times the modulating signal frequency, since the currents of all the integral multiples of the triplen carrier frequency cannot exist.

2.4 Synthesis of PWM STATION using Multiconverters with Phase Shifted Triangle Carriers

It is necessary to ensure that the voltage stresses and the current loadings are evenly shared by the individual modules. Although the low order harmonics are cancelled for the composite station, the low order harmonic currents still flow in the individual converters. The study in this chapter examines the cases of L_m converters which are

combined in parallel, in series and in parallel strings of series connected modules.

2.4.1 Direct Parallel Connection

A very important property of the Phase-Shifted Triangle Carrier SPWM technique is that the amplified modulating signals in all the converter modules have the same constant gain and there is no phase shift. Thus when f_c=9 and higher so that the sideband harmonics do not interfere with the modulating signals, all the fundamental harmonic components are equal in magnitude and in phase, so that the converter modules can be connected directly in parallel. The currents through individual modules will still contain the harmonics associated with the triangle carrier frequency f_c and the sideband harmonics which must be reduced by filter inductances. As off-the-shelf transformers are relatively cheap, their leakage inductances may be used for filtering.

Fig. 2.6 shows the oscillograms of an experiment based on 4 converter modules, connected as shown in Fig. 2.5, operating at $f_c=15f_m$, which is a triplen harmonic, under the Phase Shifted Triangle Carrier Technique. The high quality current waveform of the 5^{th} trace in Fig. 2.6(b) is the sum of currents from the converter modules displayed in the upper 4 traces of Fig. 2.6(a). Although hidden by the harmonics, it is possible to appreciate the equal magnitudes and phase angles of the amplified modulating signal in the 4 traces. The period of the saw-teeth is the period of the carrier and a closer examination shows that there is a phase displacement by 1/4 of this period in the individual traces so that on summation, the harmonics are self-cancelling, leaving the amplified signal as the 5^{th} trace of Fig. 2.6(b).

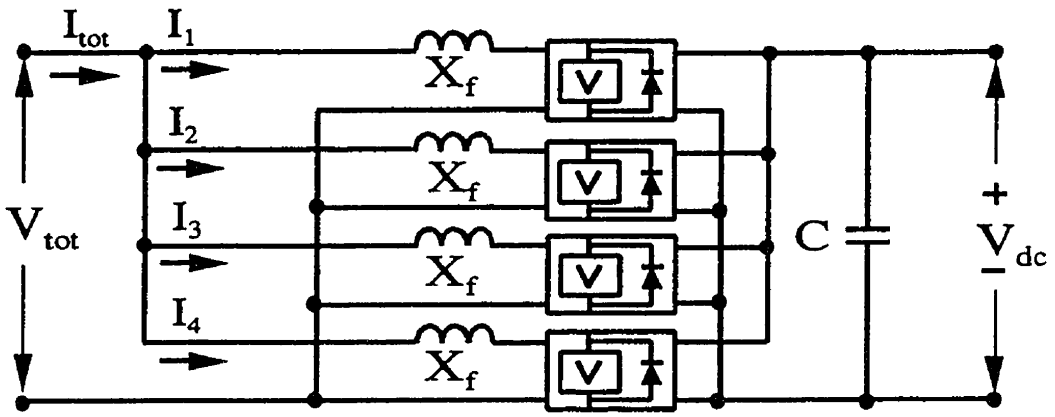


Fig. 2.5: Schematic of direct parallel connection.

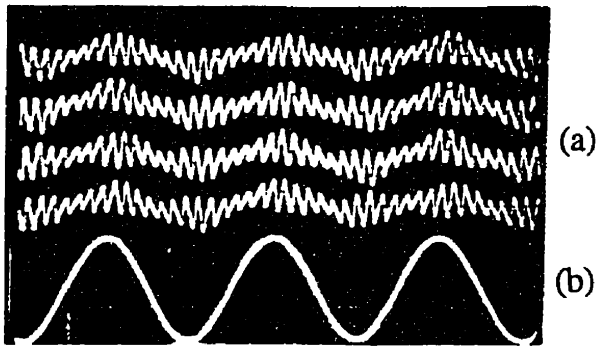


Fig. 2.6: Direct parallel connection. (a) Individual currents in the four converter modules. (b) Total current.

2.4.2 Parallel Connection using Transformers

In this connection, the ac outputs of L_m converters are connected to the secondaries of transformers and the primaries are connected in parallel to the power system. The total voltage, V_{tot}, on the output is the average of the sum of all the L_m converters scaled by turns ratio. The total current is of the same waveform quality as for direct parallel connection scaled by the turns ratio.

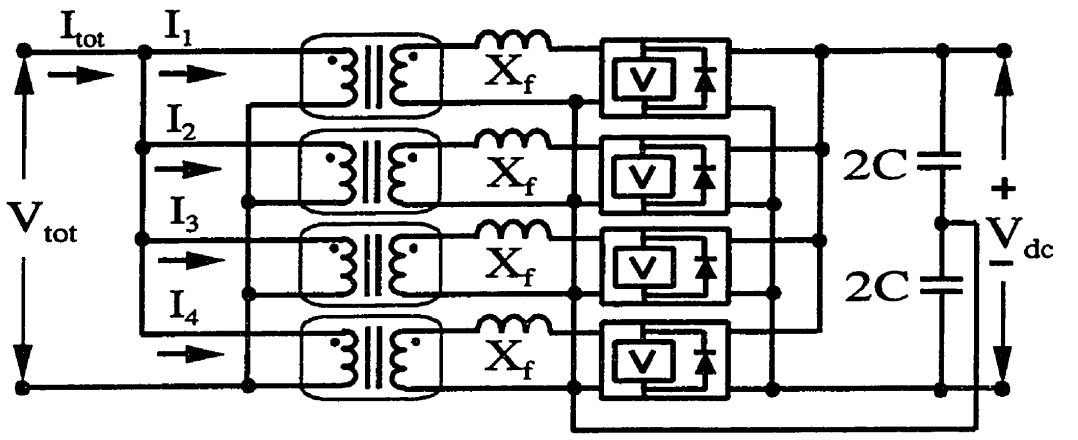


Fig. 2.7: Schematic of parallel connection using transformers with closed neutral return on the converter side.

The currents through the individual converter modules will depend on the connections of the transformer windings on the converter side. The first case is when the windings on the converter side are connected in wye and the neutral returns are connected to the mid-point of the dc link voltage as illustrated in Fig. 2.7. In this case the currents flowing through the modules are identical to the case of direct parallel connection shown in Fig. 2.6.

Another case is the open wye or delta connection of the windings on the converter side as shown in Fig. 2.8. In this case, all the triplen harmonic currents will cancel. As a result, the currents through individual converters will be of high quality as shown in Fig. 2.9(a). The open neutral connection does not allow the triplen harmonic currents to flow. The reduction of the saw-teeth of Fig. 2.6 to Fig. 2.9 means that the filter inductance size can be reduced.

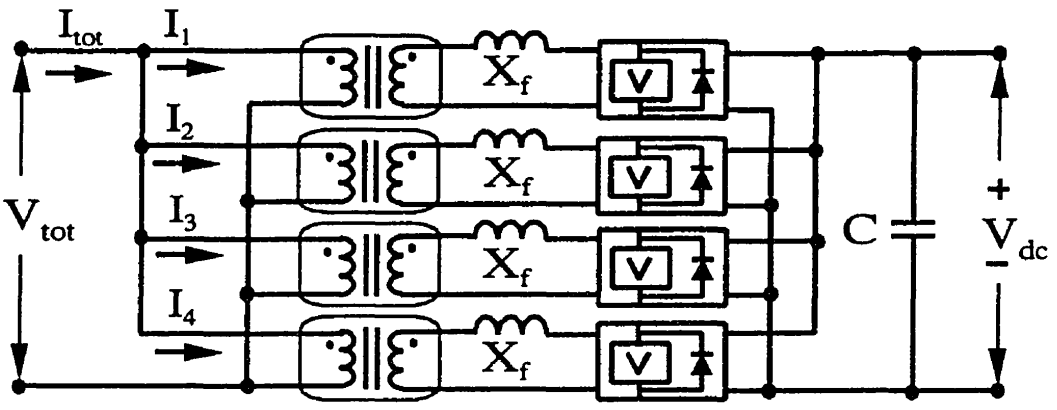


Fig. 2.8: Schematic of parallel connection using transformers with open neutral return on converter side.

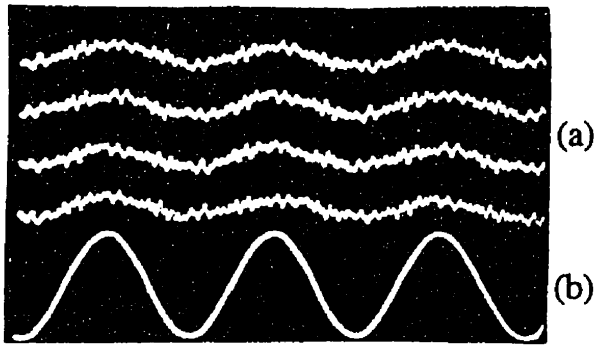


Fig. 2.9: Parallel connection using transformers with open neutral return. (a) Individual currents in the four converter modules. (b) Total current.

2.4.3 Series Connection using Transformers

In the connection of Fig. 2.10, the ac outputs of L_m converters are connected to the secondaries of transformers and the primaries are connected in series. The total output voltage is the summation of all the L_m converters (scaled by turns ratio). The current on the secondaries will be identical to the primary current (scaled by the turns ratio). From the filtering viewpoint, the series connection is better than the parallel connection as the

harmonic cancellations take place as voltages in series rather than as currents in parallel. As a result, smaller filtering inductances can be used as compared to parallel connection.

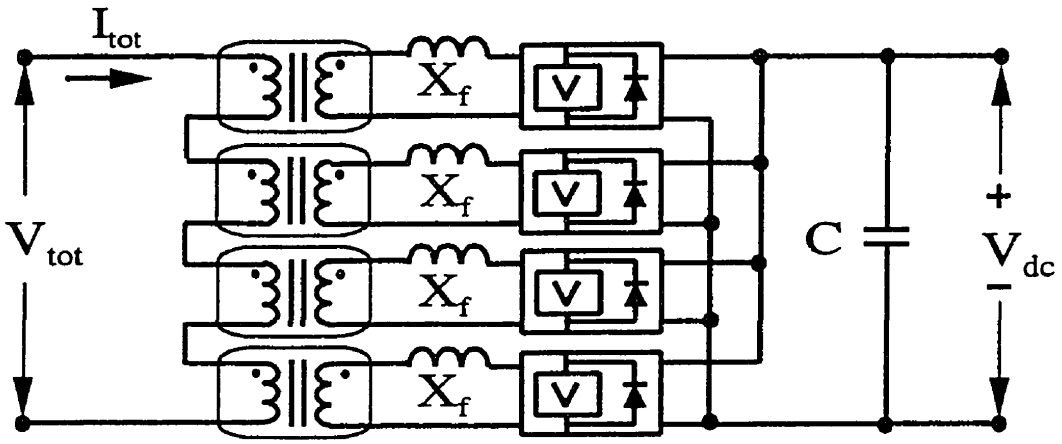


Fig. 2.10: Schematic of series connection using transformers.

Fig. 2.11 is the result of a test similar to that of Fig. 2.6 and 9, except that the transformer primaries are connected in series. The currents in all the 4 upper traces (Fig. 11(a)) are identical to the 5th trace (Fig. 11(b)) except for the turns ratio scaling factor. The series connection offers a very attractive method of integrating the multiple modules as the currents flowing through the transformers are free of harmonics.

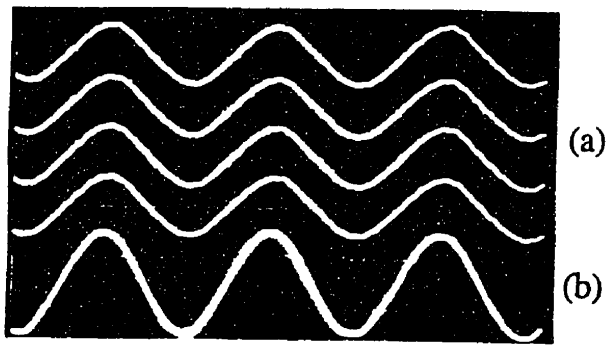


Fig. 2.11: Series connection using transformers. (a) Individual currents in the four converter modules. (b) Total current.

2.4.4 Parallel Connection of series Transformers

In the series connection, the emphasis is placed on keeping the sum of transformer primary voltages low so as to reduce insulation cost. Another objective is to use off-the-shelf transformers whenever possible, and this requires a flexibility which can be handled by parallel connections of series connected transformers as shown in Fig. 2.12(b), which illustrates the connection of 4 modules as 2 parallel strings of 2 series connected converters.

Four modules of 5kVA size 3-phase IGBT voltage source converters have been used to test the configuration shown in Fig. 2.12(b) for the test condition f_m=60Hz and f_c=540Hz. Fig. 2.13 displays the oscillograms for the test circuit of Fig. 2.12(b). From the branch currents, I_1 and I_2, shown in Fig. 2.13(d) and (e), it can be seen that the carrier and its sidebands have been eliminated in the total current shown in Fig. 2.13(f).

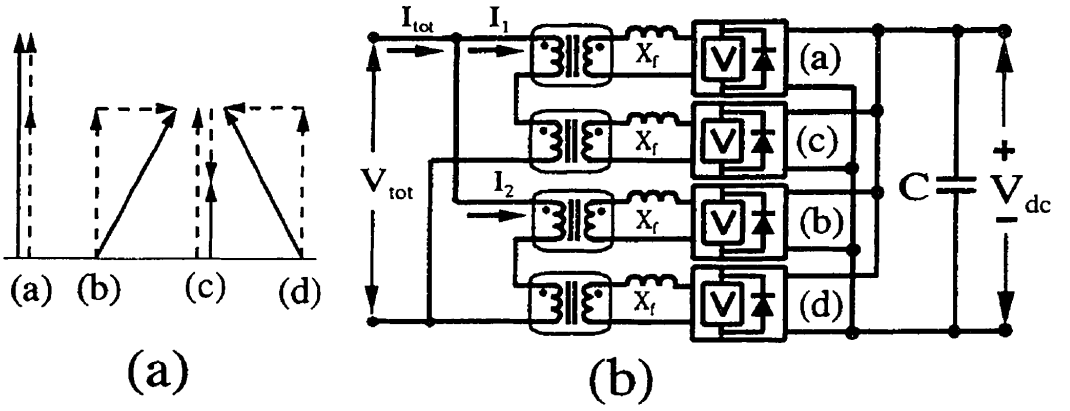


Fig. 2.12: (a) Phasors of the SPWM outputs for 4 modules. (b) Parallel connected series paired modules.

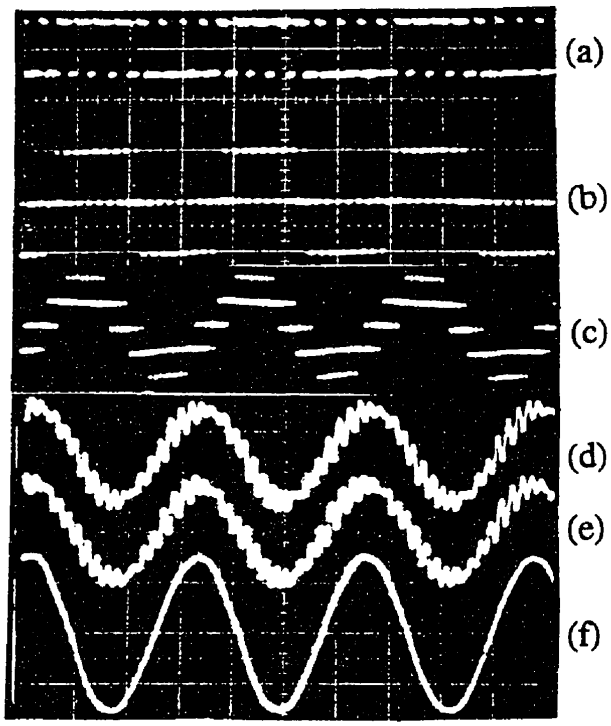


Fig. 2.13: Parallel connection of series transformers. (a) Ac output of 1 module. (b) The sum from 2 modules forming the pairs. (c) The total output voltage from 4 modules. (d) Current through 1st series connected pair. (e) Current through 2nd series connected pair. (f) Total current.

2.5 Significance of Series Connected Converter Groups at Very Low Switching Frequency

When a switching rate of 3 pulses per 60 Hz cycle is chosen [46], direct parallel connection of the multiconverter outputs is not viable. This is because from Fig. 2.3 the lower sideband of the switching noise has the frequency $f_c-2f_m=60$ Hz, which is the same frequency as the amplified modulating frequency [67,12]. Using 4 converters at a switching rate $f_c=3f_m$, the 60 Hz voltage components are illustrated in the 4 phasor diagrams in Fig. 2.12(a). The amplified fundamental modulating signals are represented by vertical broken line phasors. They are all of equal magnitude and direction. The lower

sideband voltage phasors are each displaced by 360/4=90° and are shown as broken line phasors having equal magnitudes but each phasor pointing to one of the 4 directions [35,36]. The solid-line resultants representing the unequal 60 Hz voltages in the 4 modules will result in a serious current unbalance when the 4 converters are connected in parallel. The lower sideband f_c-$2f_m$=60 Hz of the switching noise voltage can be cancelled by series connection of (a) to (c) and (b) to (d) as shown in Fig. 2.12(b).

Research based on digital simulations on a STATCOM made up of 8 and 16 converters connected in 4 parallel sets of transformer series connected converters has been pursued to verify this property. Fig. 2.14(a) shows the rms currents I_1, I_2, I_3 and I_4 in the 4 parallel branches of 2 series transformer connected converters plotted against the modulation index (M.I.). From M.I.=0.6 to 0.8, the currents are equally shared showing that the mode of cancellation of the sidebands by pairing converters is effective.

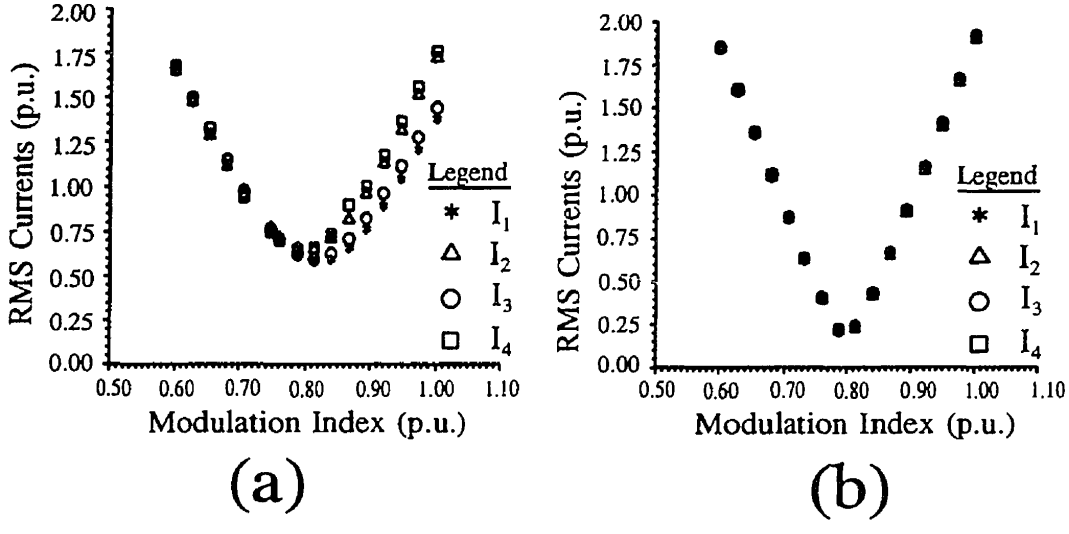


Fig. 2.14: Current sharing in 4 parallel branches of series connected converter modules, $f_c = 3f_m$. (a) 8 modules, 2 modules per branch. (b) 16 modules, 4 modules per branch.

However, when Modulation Index (M.I.) exceeds 0.8 p.u., another current unbalance due to the lower sideband $2f_c$-$5f_m$=60 Hz emerges [12]. The phasors of the lower sidebands of $2f_c$-$5f_m$ are also of equal magnitude but equally spaced out in 720 degrees. In order to ensure a complete elimination of 60 Hz voltage unbalance at 3 pulses per 60 Hz period, 4 converters have to be connected in series. One has to pair converters which eliminate the sideband of f_c-$2f_m$ and then look for the pairs which eliminate the sideband of $2f_c$-$5f_m$ also and connect them in series. The groups of 4 series connected converters are then connected in parallel. Fig. 2.14(b) shows the 4 rms branch currents from a STATCOM made up of 16 converters operating as 4 series transformer connected strings. The elimination of the sidebands of f_c-$2f_m$ and $2f_c$-$5f_m$ is complete as the 4 sets of rms currents are almost coincident.

2.6 Experimental Verification of Multiconverters with Phase Shifted Carriers at f_c=3f_m

Six modules of 5kVA size, 3-phase IGBT voltage source converters have been built for the purpose of verifying the digital simulation studies on multiconverters with phase shifted carriers [35,36]. Fig. 2.15 and 16 displays the results obtained from the series connected transformer primaries of Fig. 2.10 for the test condition of f_m=60 Hz and f_c=180 Hz, using 18 single phase transformers. Fig. 2.15 is for open neutral wye-connected transformer secondaries. Fig. 2.16 is for delta connected transformer secondaries, a configuration which allows zero-sequence to flow in the primaries. The 3 waveforms are: (a) the voltage across a transformer secondary, (b) the voltage of the sum of 6 transformer primaries, and (c) the primary line current.

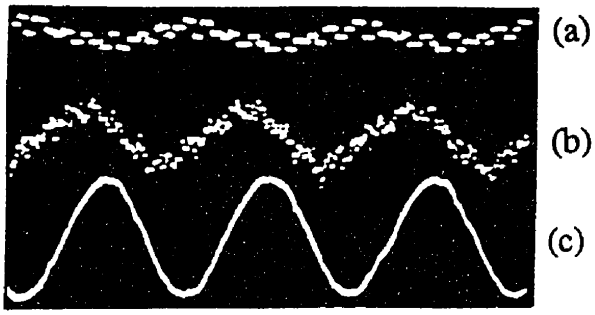


Fig. 2.15: Series connection of 6 converters with open neutral wye-connected transformer secondaries. (a) Voltage across a transformer secondary for 1 module. (b) Voltage of the sum of 6 transformer primaries. (c) Primary line current.

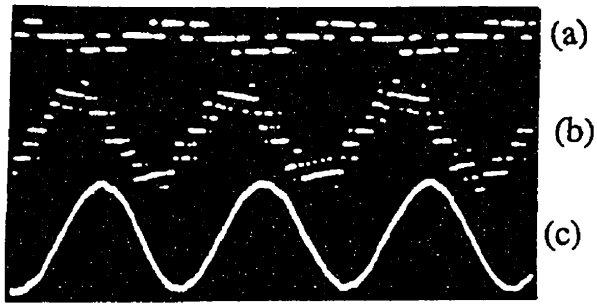


Fig. 2.16: Series connection of 6 converters with delta connected transformer secondaries. (a) Voltage across a transformer secondary for 1 module. (b) Voltage of the sum of 6 transformer primaries. (c) Primary line current.

2.7 Discussions

This study has been devoted to providing data on the characteristics of the different ways of connecting the multi-modules. The final decisions are left to the manufacturers who are more knowledgeable, especially regarding the sizes of off-the-shelf transformers available. From the point of view of insulation costs, the number of transformers to be connected in series should be kept low. On the other hand, copper losses are low when the voltage ratings are kept high.

The core losses in the transformer intermagnetic stage must also be factored in.

From [71], the core losses are proportional to $(kI_k)^2$ where k is the harmonic number. The excellent current waveforms in Fig. 2.15 and 16 indicate that the series connection is advantageous. The delta connection of the transformer secondaries in the connection of Fig. 2.16 allows zero sequence currents to flow in the primaries. In transmission line practice, it is necessary to provide a path for the zero sequence currents during faults.

It is necessary to explain why two transformer stages are proposed and why the primary winding turns are not chosen so that the voltages of their series connections reach the transmission line voltage ratings, thus foregoing the second step-up transformer stage. It has been explained to the authors that insulation co-ordination especially during switching transients and protective relay considerations require extensive studies before the single transformer stage based on series connected primaries can be approved.

2.8 Summary

Simulation studies based on shunt PWM-SVC have shown that, at $f_c = 3f_m$ switching rate, 4 series connected converters are adequate to form one group for equal load current sharing among the converter modules. The series connected converters are chosen in such a way that the low order switching noise cancel. The groups can then be connected in parallel to obtain high current rating and greater reliability. The phase shifted triangle carrier SPWM method can be used to synthesize high power FACTS controllers where the GTOs can operate at as low a switching rate as $f_c = 3f_m$.

The next chapter presents the 7-Timer Method of controlling multiconverters operated with phase shifted triangle carriers using digital controller. The Method has been tested by simulations and confirmed experimentally using 4 and 6 modules of converters.

CHAPTER III

DIGITAL IMPLEMENTATION OF PHASE SHIFTED TRIANGLE CARRIER TECHNIQUE OF SINUSOIDAL PULSE-WIDTH MODULATION (SPWM) STRATEGY

3.1 Introduction

Chapter II has shown how multiple modules of the 2-level, 3-phase voltage source converters have the characteristics of high power, linear amplifier when operated under the phase-shifted, triangle carrier technique of the sinusoidal pulse width modulation strategy [35,35,72]. One remaining challenge consists of finding a fast, accurate method of digitizing the technique.

This chapter reports on the research aimed at achieving digital control of the high power electronic converters. The digitally controlled converters have applications as ac power supplies (from large battery or fuel-cell storage) [73,74], and as FACTS (Flexible AC Transmission Systems) controllers: such as shunt STATCOMs (STATic COMpensators) [25,75], series STATCOMs [27,76] and UPFCs (Unified Power Flow Controllers) [28,77].

The high power converters, especially the FACTS controllers, have been expected to play important roles in dynamic performance enhancement, stabilization, and active filtering, in the electric utility environment. The high linear amplifier gain and high power capability mean that many of the useful methods of classical and modern control and active filter theories can be channelled through the FACTS controllers to fulfil these roles [78]. However, many of the sophisticated control strategies require real-time computations

which must be performed by fast digital signal processors (DSPs), singly or in parallel.

Hitherto, the application of computer control in power electronics has necessitated the translation of the "natural sampling" of the SPWM strategy to the "regular sampling" of the 4-Timer Method [68]. This chapter modifies the essential ideas behind the 4-Timer Method, which was developed for a single, 3-phase inverter unit, so that the array of N modules of 3-phase bridge converters can be controlled by the phase-shifted triangle carrier technique of the SPWM strategy. This modification is realized in its final form under the name "7-Timer Method", which is described in this chapter.

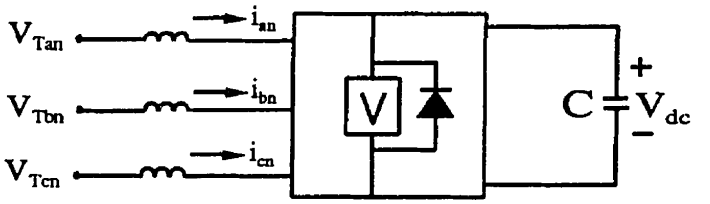
Both the 4-Timer and the 7-Timer Methods take regular periodic samplings and use the sample-and-hold data as the modulation signals in the predictions of the pulse widths in the SPWM strategy. The 7-Timer Method has a fast and accurate sampling method, which is compatible with the high effective carrier frequency Nf_c, even though the individual converter must operate at a low pulsing rate, f_c, because the high power solid-state switches are inherently slow.

In the writing of the chapter, the Sinusoidal Pulse Width Modulation and the Phase-shifted Triangle Carrier Technique are first reviewed briefly in the context of "natural sampling". The 7-Timer Method is then presented as a translation of "natural sampling" to "regular sampling". Digital simulations and laboratory experiments demonstrate the effectiveness of the Method.

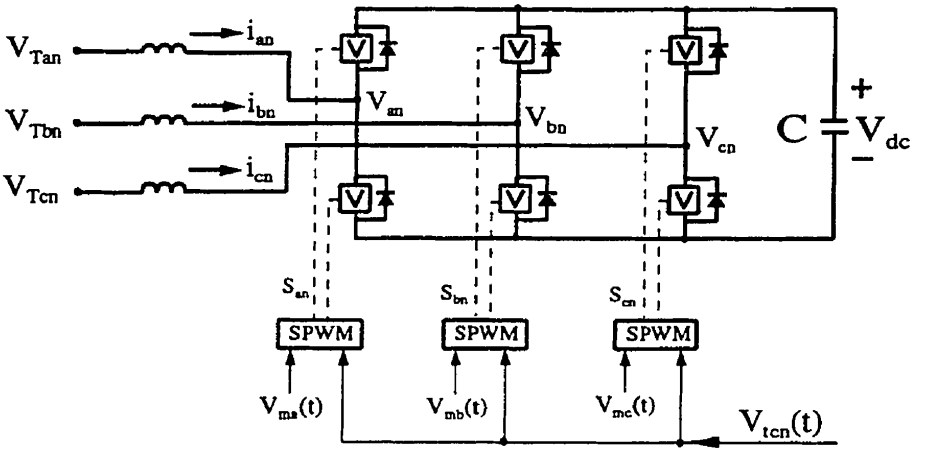
3.2 Multi-converter Array

In this chapter, Fig. 3.1(a) is the symbol representing the 3-phase, voltage-source

bridge converter of Fig. 3.1(b). Fig. 3.2 shows the general method of connecting the M_c rows of converter modules in series, and N_c columns of converters in parallel. The ac-terminals of the N (=M_c x N_c) converters are connected to transformers. The series connections increase the dc voltage across D and E. The parallel connections increase the ac current rating.



(a)



(b)

Fig. 3.1: 3-Phase Voltage Source Converter. (a) Symbol. (b) Schematic.

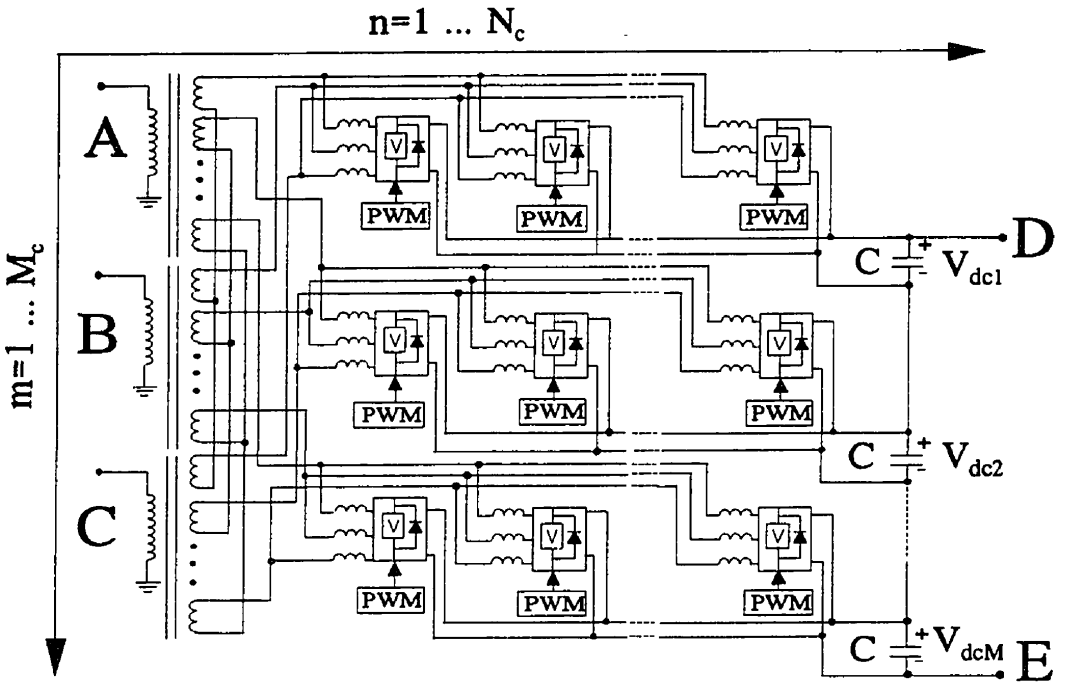


Fig. 3.2: System of Multiconverters.

3.3 Natural Sampling

3.2.1 Sinusoidal Pulse Width Modulation (SPWM)

Fig. 3.3(a) illustrates the Sinusoidal Pulse Width Modulation method based on using the intersection points of the modulation signal $V_m(t)$ and the triangle carrier signal, $V_{tc}(t)$, as the time instants for turning the switches in a given phase, complementarily ON and OFF. This method of encoding the modulating signal through the pulse width, is accurate when the frequency of the carrier, f_c, is sufficiently high. The modulation signal is amplified with a constant gain, without delay.

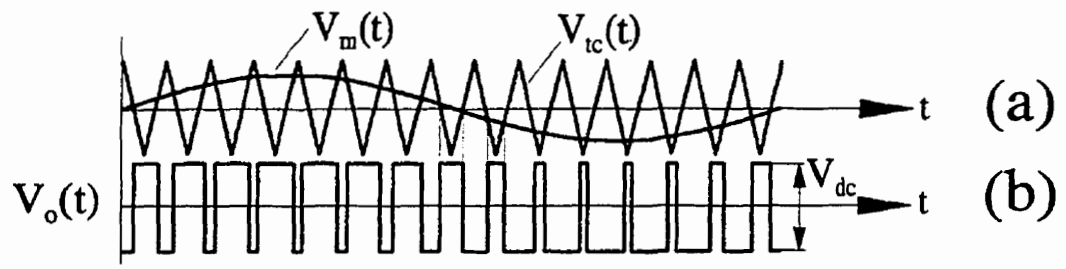


Fig. 3.3: Sinusoidal Pulse Width Modulation. (a) Modulating Signal and Triangle Carrier. (b) PWM Output Voltage.

3.2.2 Phase-Shifted Triangle Carrier Technique of SPWM Strategy

In applying the phase-shifted triangle carrier technique to the SPWM strategy to control the multi-converter array of Fig. 3.2, each phase of all the N modules receives the same modulating signal $V_m(t)$ through a SPWM black-box in Fig. 3.1(b). However, in each module (n=1,2...N), the black-box receives its individual triangle carrier signal, $V_{tcn}(t)$. The carrier signals are identical triangles, except for the phase shifts based on dividing the carrier period $T_c=1/f_c$ by N, Mathematically, the n^{th} carrier $V_{tcn}(t)$ is related to the first carrier $V_{tc1}(t)$ by:

$$V_{tcn}(t) = V_{tc1}[t - (n-1)T_c/N] \qquad n = 1, 2, \ldots N \tag{3.1}$$

Fig. 3.4(a) illustrates the phase-shifted carrier waveforms and the modulation waveform. The SPWM black-box of Fig. 3.1(b) in each module compares the modulating signal with its phase-shifted carrier. Fig. 3.4(b) and (c) illustrate how the pulsed outputs of two converters are staggered because the same modulating waveform intersects the phase-shifted carriers at different instants. The output of one phase of the array consists of the summation of N pulsed waveforms of the forms of Fig. 3.4(b) and (c).

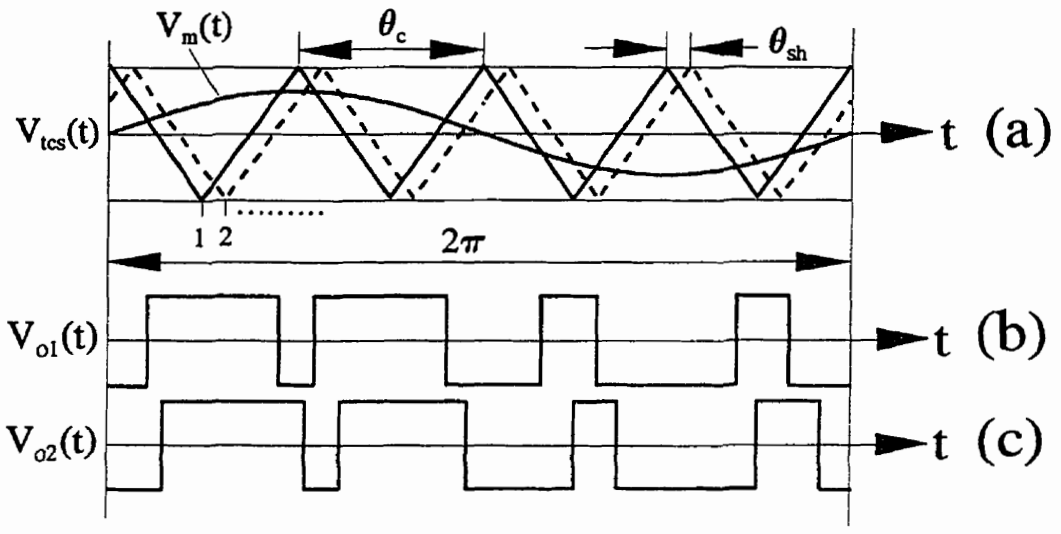


Fig. 3.4: Phase Shifted Triangle Carrier Technique. (a) Modulating Signal and Phase Shifted Triangle Carriers (n=1,2). (b) PWM Output for the First Converter (c) PWM Output for the Second Converter.

For testing purpose, the modulation waveform in Fig. 3.5(a) consists of the 1st, 3rd, 5th and 7th harmonics of the Fourier decomposition of the square wave. This waveform has been chosen so that comparison with the output enables a quick recognition that the linear amplifying property is indeed accomplished through the phase-shifted triangle carrier technique of the SPWM strategy. Fig. 3.6(a) is the Fast Fourier Transform (FFT) of Fig. 3.5(a), showing the 1st, 3rd, 5th and 7th harmonics. Fig. 3.5(b) shows the output pulsed waveform of one of the 24 converters. The carrier-to-modulation frequency ratio, $f_c / f_m = 5$. Fig. 3.5(d) shows the summation of output waveforms of 24 converters. It is evident that the output in Fig. 3.5(d) is an excellent replica of the input waveform of Fig. 3.5(a), which is a consequence of the high effective carrier frequency, which is $Nf_c = 120 f_m$ Hz.

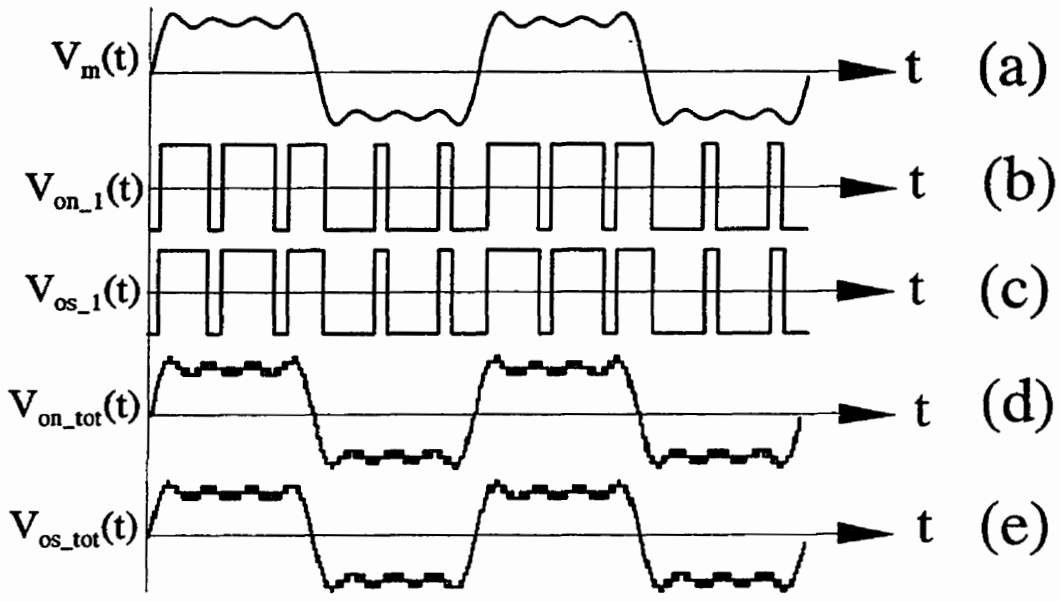


Fig. 3.5: Simulated results. (a) Truncated square wave input signal. (b) Natural sampled PWM output for 1-converter. (c) Regular sampled PWM output for 1-converter. (d) Natural sampled PWM output for 24-converters. (e) Regular sampled PWM output for 24-converters.

3.4 Regular sampling

The naturally sampled SPWM as illustrated in Fig. 3.7(a), requires the commitment of at least one DSP to monitor the modulation signal and the triangle carrier signal continually, in order to detect the time instants when they are equal at t_{on}, t_{off}, whereupon commands are issued in real time to execute the switchings. By making use of regular sampling, the DSP can be freed to perform computational functions, including the computation of the switching times which are then loaded onto counters.

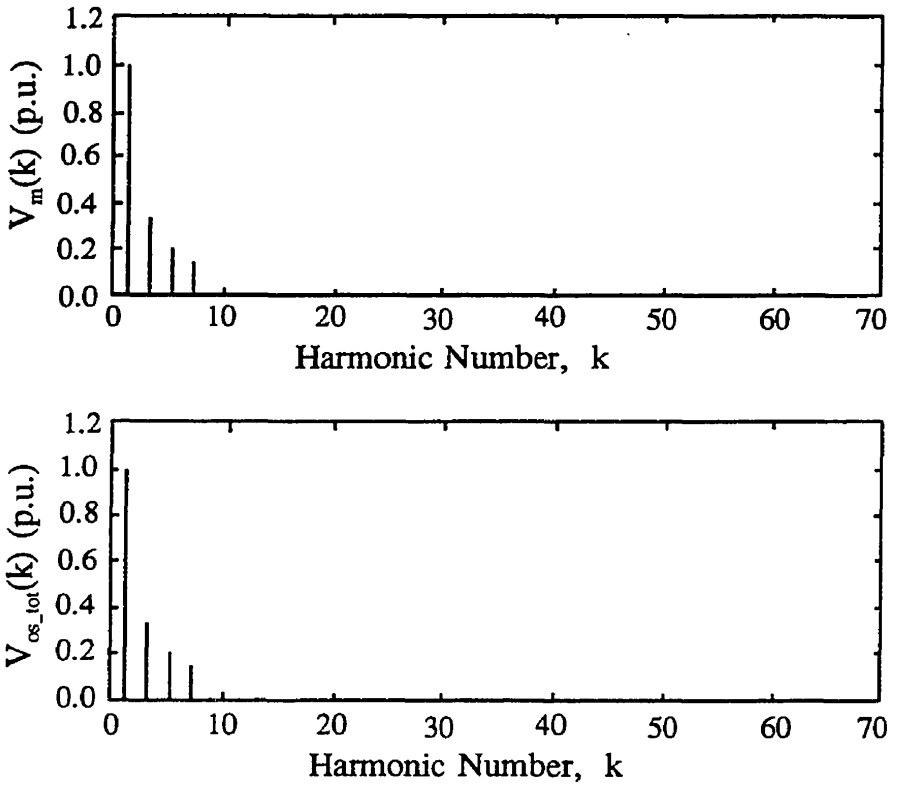


Fig. 3.6: Fourier series of simulated results. (a) Spectrum of truncated square wave input Signal. (b) Spectrum of Regular sampled PWM output for 24-converters.

Fig. 3.7(b) illustrates the method of applying regular sampling to the SPWM strategy. The sampling instants are taken at the extrema points of the triangle carrier. The sampling frequency is $2f_c$ and the sampling period is $T_s=1/(2f_c)$. Applying sample-and-hold, the original modulation signal, $V_m(t)$, becomes the stepped waveform, $V_{ms}(t)$. The SPWM method is applied next, using the intersection points of the triangle carrier signal $V_{tc}(t)$ and the sample-and-hold signal $V_{ms}(t)$ as the switching instants. The advantage is that at each sampled instant, the switching times t_{on} and t_{off} can be computed

from the properties of similar triangles, since $V_{ms}(t)$ is held constant in the sampling period T_s.

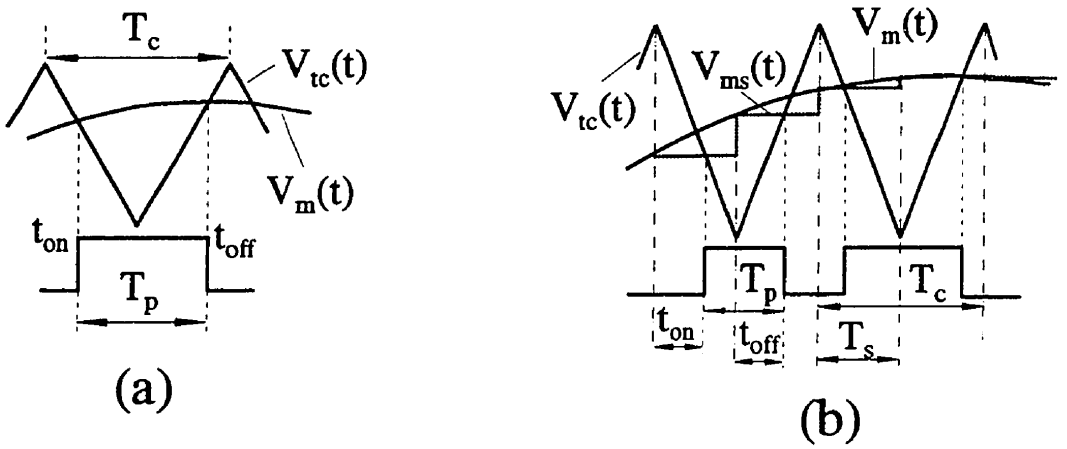


Fig. 3.7: (a) Natural sampled SPWM (b) 4-Timer Method of Regular sampled PWM.

In digital control, the computed values "t_{on}" and "t_{off}" are then loaded onto the registers of "electronic timers", which are external to the DSP. After the clocking times are found to be equal to the allotted times, commands are sent to the base drives of the converter phases to execute the ON or OFF commands. The duty-time of the DSP to accomplish the sampling and the computation of t_{on}/t_{off} is minimal and the remaining time can be used for other duties. The accuracy of the regular sampling method is good when f_c is high, as the pulse width T_p of Fig. 3.7(b) approaches that in Fig. 3.7(a).

3.4.1 4-Timer Method

The 4-Timer Method is the implementation of the SPWM strategy, based on translating natural sampling to regular sampling. One timer is used for each of the 3 phases. The times "t_{on}" and "t_{off}" are computed, alternately using the ascending and the

descending sides of the triangle carrier. The fourth timer keeps track of the sampling time T_s.

3.4.2 Poor Accuracy from Low Triangle Carrier Frequency f_c

At the off-set, the computer control by the phase-shifted triangle carrier technique of the SPWM strategy seems to be a simple matter of using 3N+1 timers. Unfortunately, accuracy would be a problem. As high power solid-state switches are generally slow so that a low triangle carrier frequency f_c must be used to reduce switching loss, poor accuracy is to be expected in applying the regular sampling method, exemplified by Fig. 3.7(b).

3.5 Triangle carrier grid

Since the 7-Timer Method is based on mimicking the phase-shifted triangle carrier technique as closely as possible, some familiarity with the patterns of the phase-shifted triangle carriers helps in the understanding of the ideas involved. To meet this objective, Fig. 3.8 presents the grid of phase-shifted triangle carriers for: N=2 converters in (a), N=4 converters in (b), and N=6 converters in (c). In this study, N, the number of converters considered must be even, as the upper triangle apexes are coincident in time with the lower triangle apexes, which offers an easier symmetry for the development of the algorithm. This insistence is not restrictive, since an even N is a preferred design choice, because the carrier switching noise at the frequencies of Nf_c, $2Nf_c$, $3Nf_c$,....do not exist when N is even.

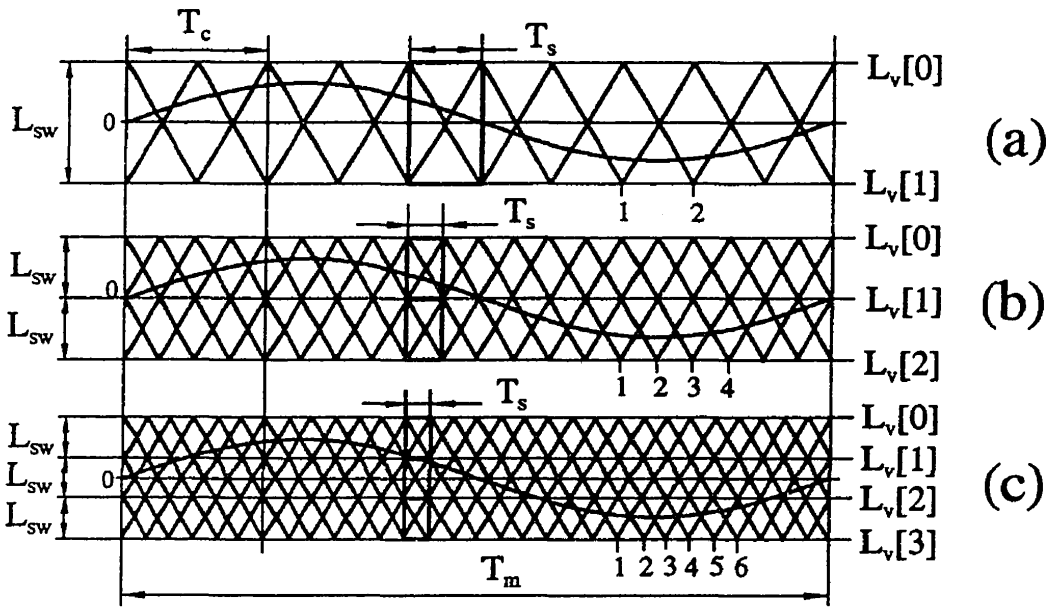


Fig. 3.8: Synthesis of Regular Sampled PWM for Multiconverters with Phase Shifted Triangle Carriers. (a) Two Converters. (b) Four Converters. (c) Six Converters.

3.5.1 Cells of Crossed-Diagonals

By comparing the grids of the triangle carrier waveforms of Fig. 3.8(a), (b) and (c), one recognizes that a repeated, basic element consists of a cell of crossed-diagonals, bounded by the sides labelled T_s and L_{sw}. The cells are numbered horizontally, left to right, using the index k, and vertically downwards, using the index i=0,1,2,..(N/2). The diagonals of each cell belong to two of the converters of the array n=1,2,3,..N. The diagonal with a negative slope belongs to the "turn-on " portion of a triangle carrier, while the diagonal with the positive slope belongs to the "turn-off " portion of another converter. For each cell, indexed as (i,k), two simple formulas (eq. 3.6 and 3.8) exist to identify the converters $n=n_{on}$ and $n=n_{off}$ to which the descending and ascending diagonals belong.

As will be seen later, it is within the cells of crossed-diagonals that the natural sampling procedure described by Fig. 3.7(a) is translated to regular sampling in Fig. 3.7(b).

3.5.2 Sampling Period, T_s

The sampling periods $T_s=1/Nf_c$, which are labelled in Fig. 3.8(a), (b) and (c), are the phase-shifts between the triangle carriers expressed in time. The sampling periods are indexed by k=0,1,2,3,...,N-1,0,1,2,3,...,N-1,0,1,2.. indicating that the count repeats with k=0,1,2.. every time the index k reaches N. As a reference, the time period of the triangle carrier $T_c=1/f_c$ is illustrated in Fig. 3.8(a).

3.5.3 Modulation Depth, L_{sw}

The number of cells, N_{c1}, along the ordinate is:

$$N_{c1} = N/2 \tag{3.2}$$

The cells are indexed by i=0,1,2,..,N_{c1}. Taking A_c to be the amplitude of the triangle carrier, the modulation depth is:

$$L_{sw} = 4A_c / N \tag{3.3}$$

The cells divide the "modulation space" into several levels labelled as $L_v[i]$ in Fig. 3.8, where:

$$\begin{aligned} L_v[i] &= (N/4 - i)L_{sw} \\ i &= 0, 1, 2, \ldots, N_{c1} \end{aligned} \tag{3.4}$$

3.6 Regular Sampling within Crossed-diagonals Cell

Fig. 3.9 depicts a modulation signal, $V_m(t)$, which changes slowly with respect to the framework of the crossed-diagonals cells (indexed i,k). In natural sampling, the

switching instants are the intersection points of $V_m(t)$ and the triangle carriers. The turn-on and turn-off instants are based on the descending and ascending slopes of the triangles respectively. The converters executing the turn-on and turn-off are identified with the triangle carriers assigned to them. Thus, they follow a cyclic sequence n=0,1,2,...(N-1), 0,1,2,...(N-1), 0,1,2,..

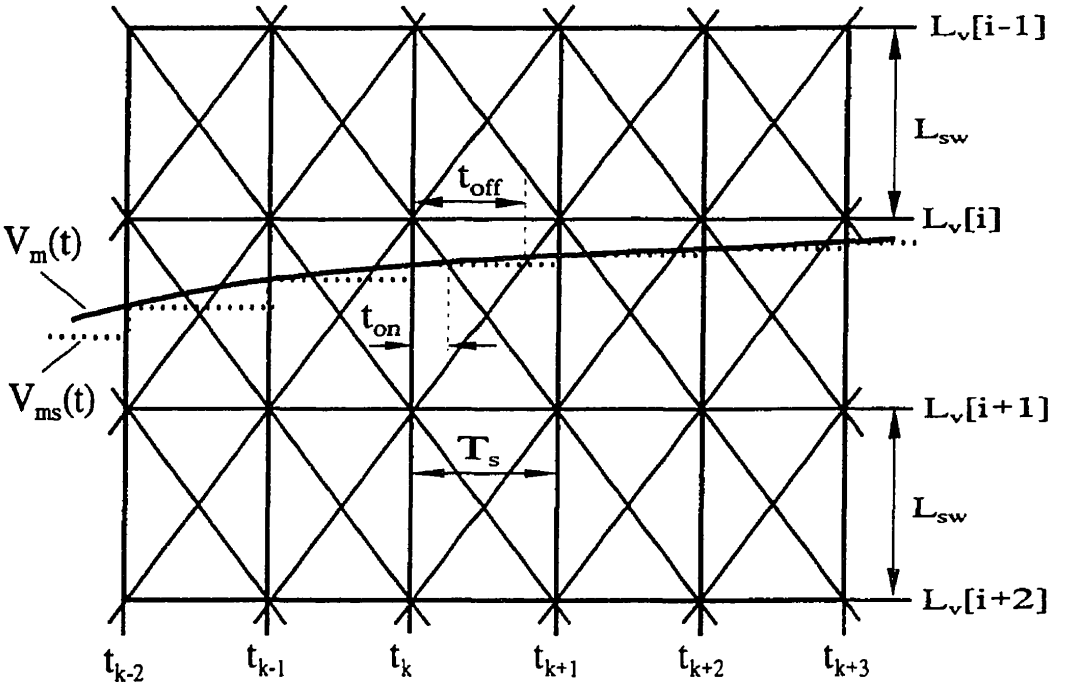


Fig. 3.9: Determination of the Switching Times (t_{on} & t_{off}) and the Switching Converters at the k^{th} Sampling Instant within the Triangle Carrier Period, T_c.

Taking regular samplings from the left-hand-side of each cell, the sample-and-hold signal, $V_{ms}(t)$ is shown as the dotted line, generated at each sampled instants, .., t_{k-2}, t_{k-1}, t_k, t_{k+1}, t_{k+2}, t_{k+3}, ... From visual inspection, it is evident that the intersections of the phase-shifted triangle carriers with the sample-and-hold $V_{ms}(t)$ are very close to the intersections with the original modulation signal $V_m(t)$, when the sampling period,

$T_s=1/(Nf_c)$, is sufficiently fine.

Based on imitating natural sampling, the algorithm of regular sampling proceeds along the following steps:

Step 1: ***Identify index k***

After the sampling-time counter has measured out the sampling period T_s, the index k-1 is incremented to (k-1)+1=k.

Step 2: ***Sample $V_m(t)$***

Upon sample-and-hold, the value $V_{ms}(t_k)$ is obtained.

Step 3: ***Identify index i***

$V_{ms}(t_k)$ fits in the index i when it lies between the levels $L_v[i]$ and $L_v[i+1]$. In principle, a comparative search is made iteratively through $i=0,1,2,..,N_{cl}$. In practice, the computation time is reduced by beginning from the value obtained from the previous sample, i[k-1]. In the example of Fig. 3.9, i[k]=i[k-1] throughout, as the modulation signal remains within the same two levels. Thus the search time is minimal. The indices (i,k) specify the crossed-diagonals cell within which the switching times are computed.

Step 4: ***Compute t_{on}***

Based on the property of similar triangles, the intersection of the descending diagonal and $V_{ms}(t_k)$ in the (i,k) cell, yields the turn-on time:

$$t_{on} = \frac{T_s}{L_{sw}}[L_v[i] - V_{ms}(kT_s)] \qquad i = 0,1,2,....,(N_{cl} - 1) \tag{3.5}$$

The time t_{on} is loaded onto the "turn-on" register.

Step 5: ***Identify the n_{on}^{th} converter to send the turn-on instruction***

From the indices (i,k) of the cell, the converter in which the turn-on instruction is to be executed, is determined by the formula:

$$\begin{aligned} n_{on} &= (N + k - i) \; Mod \; N \\ i &= 0, 1, 2, ..., (N_{cl} - 1) \end{aligned} \tag{3.6}$$

Mod N, indicating that the count repeats with 0,1,2,..,(N-1), 0,1,2,.. every time the index (N+k-i) reaches N. n_{on} contains the remainder after (N+k-i) is divided by N. The selected routing of the instruction to the converter n_{on} is accomplished through hardware demultiplexers.

Step 6: ***Compute t_{off}***

From the ascending diagonal of the (i,k) cell, the "turn-off" time is computed:

$$\begin{aligned} t_{off} &= \frac{T_s}{L_{sw}} \left[V_{ms}(kT_s) - L_v[i+1] \right] \\ i &= 0, 1, 2, ..., (N_{cl} - 1) \end{aligned} \tag{3.7}$$

This time is loaded onto the "turn-off" register.

Step 7: ***Identify the n_{off}^{th} converter to send turn-off instruction***

The converter in which the turn-off instruction is to be executed is determined by the formula:

$$\begin{aligned} n_{off} &= (k+i+1) \; Mod \; N \\ i &= 0, 1, 2, ..., (N_{cl} - 1) \end{aligned} \tag{3.8}$$

n_{off} contains the remainder after (i+k+1) is divided by N. The hardware demultiplexer routes the instruction to converter n_{off}.

3.6.1 Problem of Skipped Converter

Unavoidably, there are occasions when within the same sampling period $[t_{k-1}, t_k]$, the modulation signal, $V_m(t)$, crosses over from one cell to another, above it as shown in Fig. 3.10, or below it as in Fig. 3.11. By comparing the intersections based on the modulation signal $V_m(t)$ with those of the dotted sample-and-hold signals $V_{ms}(t)$, it is evident that in regular sampling, one converter would have skipped a scheduled switching, marked **P**, while another converter would have received two repeated instructions in quick succession at **Q** and **R** (which is innocuous since they are identical commands separated by a brief time interval). The cross-over can only be noticed after the event, at sampling instant t_k.

The cross-over is detected at Step 3, by noting that the index i[k] has decreased (modulation signal having a positive slope) or increased (negative slope) from i[k-1] of the previous sample. The "skipped" converter is already late in executing the scheduled switching at **P**. In order to minimize the error, the scheduled switching is executed immediately. No special action needs to be taken with respect to the other converter which receives the two repeated commands.

Two unavoidable errors are incurred at each cross-over of levels. The "skipped" converter, in executing the command at t_k, is already late. The other converter in executing the first of the repeated commands, at intersection point **Q** errs on the too early side. These errors are inherent in the sample-and-hold method and can only be minimized by operating with a high sampling frequency, Nf_c.

A method, based on approximating the modulating signal by a straight line joining the samples of t_{k-1} and t_k in the $k\pm1$ cell, will improve the accuracy, but the algorithm will

be more complicated.

(i) Positive Slope Cross-Over

For the case of the cross-over by a positive slope in Fig. 3.10, the converter to which the immediate turn-on command is to be sent is:

$$n_{on} = (N + k - i - 1) \; Mod \; N \qquad i = 0, 1, 2, \ldots, (N_{cl} - 1) \tag{3.9}$$

This action replaces Steps 4 and 5.

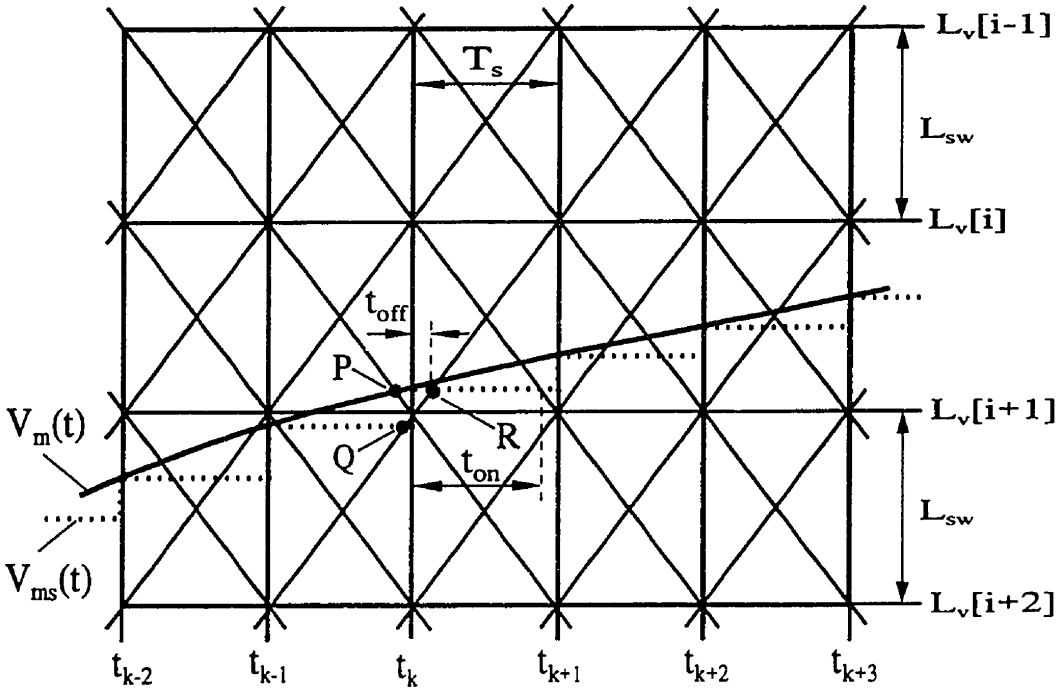


Fig. 3.10: Determination of the skipped Converter to be Switched on. The Modulating Signal crossed one Voltage Level with Positive Slope within a Sampling Period, T_s.

(ii) Negative Slope Cross-Over

For the case of negative slope cross-over depicted in Fig. 3.11, the immediate turn-off command is sent to converter n_{off}, where

$$n_{off} = (k+i)\,Mod\ N, \qquad i = 0,1,2,....,(N_{cl} - 1) \tag{3.10}$$

This action replaces Steps 6 and 7.

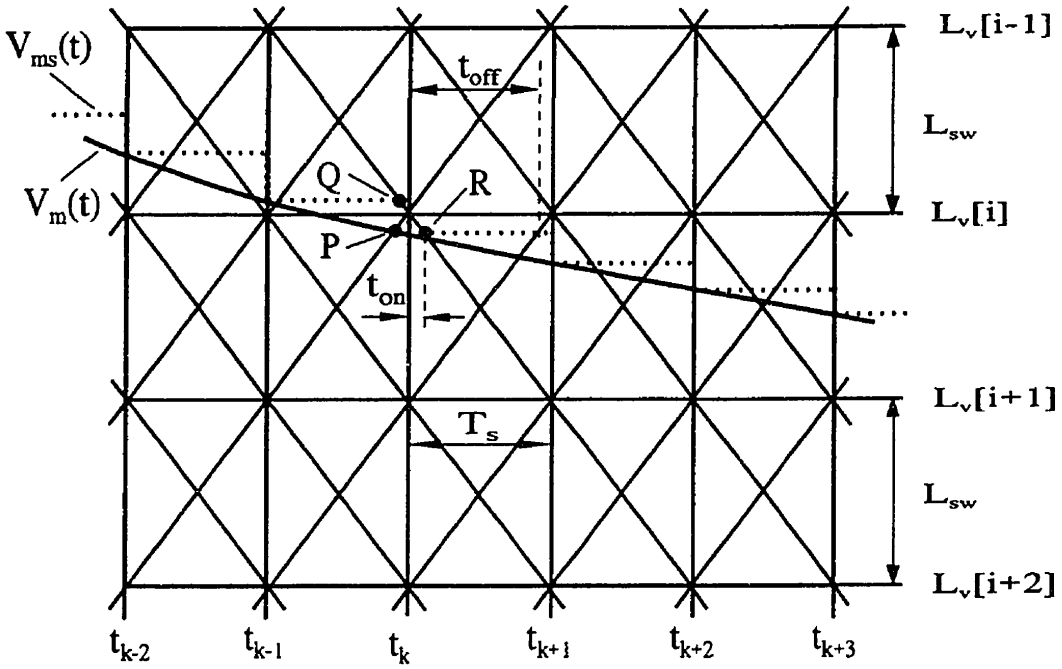


Fig. 3.11: Determination of the skipped Converter to be Switched off. The Modulating Signal crossed one Voltage Level with Negative Slope within a Sampling Period, T_s.

3.7 7-Timer Method

Step 5 and 7 reduce the number of timers required by each phase to 2, irrespective of N, the number of converters. For each phase, two timers are required for "t_{on}" and "t_{off}". Thus for a 3-phase system, a total of 7 timers are required, the 7^{th} timer being used to time the sampling period, T_s.

3.8 Simulation Studies

Off-line PC simulation studies of the 7-Timer Method have been pursued with two objectives in mind: (1) To evaluate the accuracy of the 7-Timer Method. The test signal of Fig. 3.5(a) has yielded simulation results from the naturally sampled phase-shifted triangle carrier technique, which are shown in Fig. 3.5(b) and (d). The corresponding waveforms from the 7-Timer Method are displayed in Fig. 3.5(c) and (e). The agreement of Fig. 3.5(e) with (d) and (a) are excellent. Fig. 3.6(b) is the FFT of Fig. 3.5(e), showing that the spectrum of the original test signal in Fig. 3.6(a) is reproduced by the 7-Timer Method. The simulation results of Fig. 3.5 and the FFT spectrum in Fig. 3.6 show that the 7-Timer Method yields the linear amplifier property. (2) To develop the real-time DSP codes to operate the multi-converters in the experimental tests. The same software, which has been written in C for the off-line PC simulations, after passing through the TMS320-C40 DSP C-compiler Optimizer, has been ported to run the TMS320-C40 DSPs in real-time.

3.9 Implementation of 7-Timer Method

3.9.1 Software

The software based on the algorithm described in section 3.6 was written in C, tested in the PC and proven in Fig. 3.5(e) and 3.6(b).

3.9.2 Hardware

The hardware comprises of a Texas Instruments TMS320-C40 DSP and a Field Programmable Gate Array (FPGA) device which serves as the intermediary between the

DSP and the gating circuits of the IGBT converter modules. Each of the 7 timers is made up of a magnitude comparator in the FPGA. One input port of each comparator is connected to the data bus of the clocking counter. The second input port of six of the comparators are connected to the output buses of the registers, onto which the computed times t_{on} and t_{off} of the a, b, and c-phases are loaded by the DSP after the computation of each sampling instant. The output of each comparator of t_{on} (or t_{off}) is routed to the n_{on}^{th} (or n_{off}^{th}) converter by a demultiplexer, whose register has previously been loaded with the address n_{on} (or n_{off}) by the DSP. The register of the 7^{th} comparator contains the sampling period, T_s.

3.10 Experimental Results

Six, 5kVA-size, 3-phase, IGBT, voltage-source converter modules have recently been designed and built in the power electronics laboratory for the purpose of carrying out an experimental research program on laboratory FACTS controllers based on multi-converters. The 7-Timer Method has been very successful in the DSP control of the multi-converter array and [79] contains published results of the experimental research. Two sample results are presented:

3.10.1 Test on 4 Converters, f_c/f_m=15, Parallel Connection

For f_c/f_m=15, the converter modules, operated under the 7-Timer Method (which implements the phase-shifted triangle carrier technique), can be connected directly in parallel as shown in Fig. 3.12, without serious ac current unbalance from the individual modules. Fig. 3.13(a) and (b) show the ac voltages of a single module and the composite

voltage of the 4 converters. Fig. 3.14(a) and (b) show the 4 branch ac currents with their carrier ripples and the total current in which the ripples have been annulled by harmonic self-cancellations. The equivalent carrier-to-modulation frequency ratio is $4xf_c/f_m=60$, and this is reflected in the high quality in the waveform of the total current.

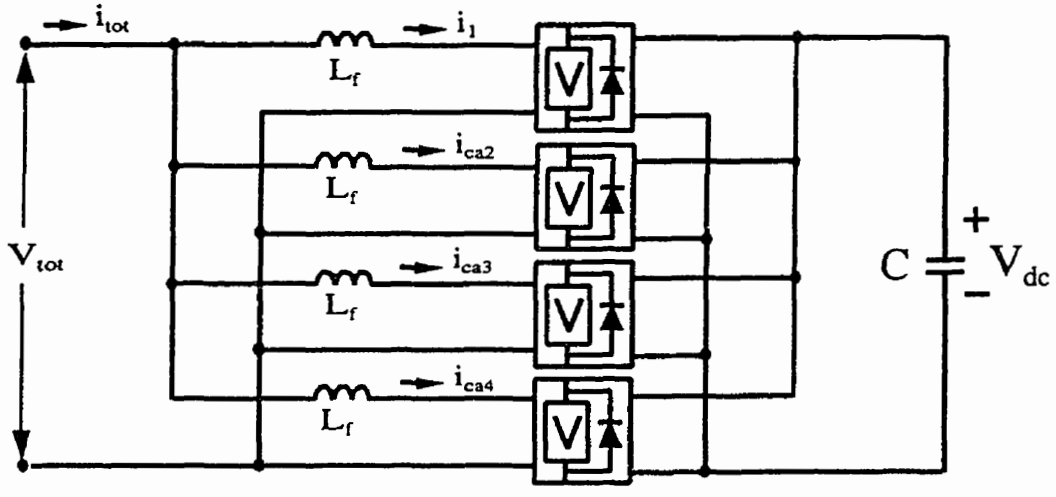


Fig. 3.12: Direct Parallel Connection of Multiconverter System.

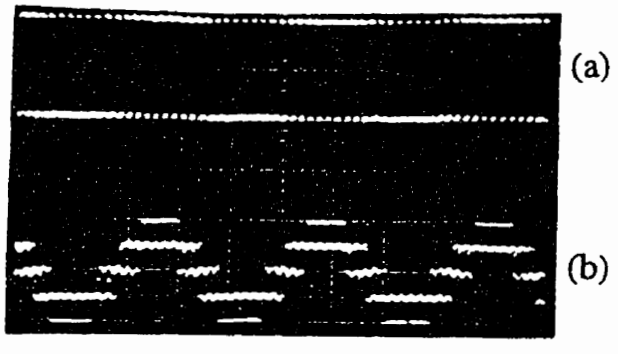


Fig. 3.13: Output Voltage Waveforms for Direct Parallel Connection.
(a) Single Converter Module. (b) Four Converter Modules.

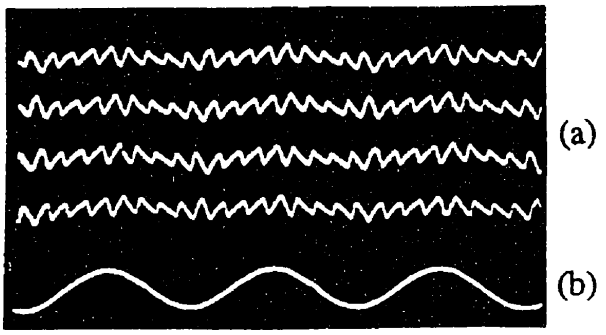


Fig. 3.14: Current Waveforms for Direct Parallel Connection. (a) Individual Currents in the 4 Converter Modules. (b) Total Current.

3.10.2 Test on 6 Converters, f_c / f_m=3, Series Connection Using Transformers

For f_c / f_m=3, the converter modules, operated under the 7-Timer Method, cannot be connected directly in parallel because the ac voltages of the individual modules are not equal. The multi-converters must be connected in series through transformers as shown in Fig. 3.15. Fig. 3.16 shows the waveforms of an experiment in which 6 converters under the 7-Timer Method feed a resistive load with small inductance (Q-Factor = 0.25). Fig. 3.16(a), (b) and (c) show respectively, the output voltage of a single module, the composite voltage at the transformer output, and the load current.

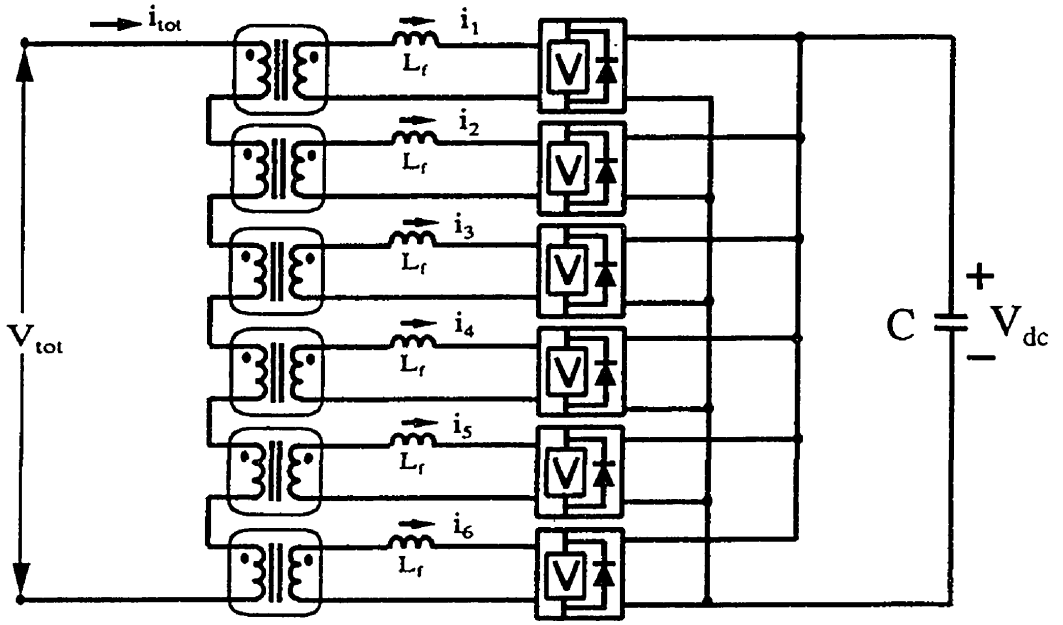


Fig. 3.15: Series Connection of Multiconverter System using Transformers.

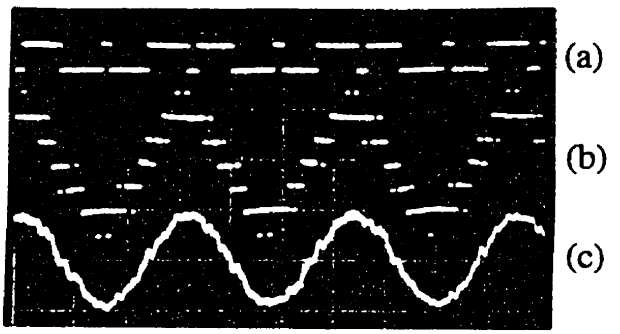


Fig. 3.16: Voltages and Current Waveforms for Series Connection of six Converter Modules at $f_c=3f_m$. (a) Output Voltage for Single Converter Module (b) Total Voltage for six Converter Modules. (c) Load Current.

The experimental results from the two sample experiments point to the 7-Timer Method as having successfully and accurately implemented the phase-shifted triangle

carrier technique of the SPWM.

3.11 Summary

In this chapter, the 7-Timer Method has been described, and the simulation and experimental results presented are proofs of its effectiveness. The 7-Timer Method enables an array of converter-modules to be operated as high power linear amplifiers of high constant gain (without phase shift), under computer control.

PART 2:

DIODE-CLAMPED MULTILEVEL CONVERTERS

CHAPTER IV

SPWM STRATEGY IN DIODE-CLAMPED MULTILEVEL TOPOLOGY: SINGLE MODULE AND MULTI-MODULES

4.1 Introduction

Part 1 has been concerned with 2-level, 3-phase voltage-source converters. The minimum switching rate is 3 pulses per cycle of the 60Hz modulation signal. A switching rate of 12 pulses per modulating cycle or higher is preferred but this is beyond the capabilities of presently available gate-turn-off thyristors (GTOs). Part 2 examines the potential of the diode-clamped multilevel topology. Under the fundamental frequency method of control, the switching rate is the minimum of 1 pulse per modulating cycle. The fundamental frequency method does not have the linear amplifier characteristics of SPWM. This chapter is concerned with implementing SPWM strategy in the diode-clamped multilevel converters.

Multilevel converters constitute the key technology of power electronics to reach the high power ratings required by controllers of Flexible AC Transmission Systems (FACTS). The 80 and 100 MVA size GTO STATCOMS which have been installed in Japan [26] and USA [25] respectively, based on 2-level converters, are examples of the manufacturers' state-of-the-art in high power electronics for the electric power utility market. The GTOs are pulsed once per line frequency cycle to minimize switching loss. Real power is controlled by advancing or retarding the ac voltage phase angle. Ac voltage magnitude is controlled by increasing or decreasing the dc capacitor voltage. Another alternative of output voltage magnitude control is by employing transformer tap changers.

A high quality sinusoidal voltage waveform is synthesized by cancellations of harmonics in 8 square-wave voltages from 8 modules of GTO converters. Two transformer stages are used. The first stage applies magnetic circuits to integrate the power from the 8 modules. The second stage steps up the voltage to the transmission line voltage levels. As discussed in [26], the first stage consists of phase-shifting transformers with the turns of the tertiary windings providing the means of designing the requisite phase shifts. Incidentally, in order to satisfy the high MVA required, the GTOs have to be connected in series and/or in parallel in order to augment the voltage/current ratings, so that the multimodules do not add to the cost.

Anticipating the near future when GTOs can switch at a faster rate, research has already begun on sinusoidal pulse width modulated (SPWM) converters as controllers in Flexible AC Transmission Systems (FACTS) [77,80]. As SPWM-controlled converters function as linear amplifiers, they are suited to handle feedback and active filtering signals, which are added to the line frequency ac template waveforms in the modulating signal.

From research on multimodules of 2-level converters connected in parallel [36] and in series [35], it has been shown that the GTOs need to switch only at 300 Hz (number of triangles per modulating cycle, $K_c = 5$) provided the "phase shifting triangle carrier technique" is adopted. When M modules are employed, the equivalent triangle carrier number is $K_{eff} = MK_c$. Thus, as broad a frequency bandwidth as is required by feedback and active filtering signals can be provided for, by the choice of M, the number of converter modules.

The introduction of the multilevel converter concept [38,39] has added impetus to

this line of research. The multilevel connection enables the ac voltage to be increased without transformers. The cancellation of low frequency harmonics from the ac voltages at the different levels means that the size of the ac inductances can be reduced.

Up to this point in time, however, research [40,42,63,64,81,82] has shown that the Fundamental Frequency Method of switching is more promising than the SPWM method in controlling the multilevel converter. For example, to obtain 5% total harmonic distortion (THD) factor in voltage, the SPWM method requires K_c = 63 carrier triangles per modulating cycle in the 5-level converter. In contrast, each GTO is pulsed only once per cycle in the Fundamental Frequency Method. Surprisingly, the SPWM multilevel converter has to switch even faster than the 2-level converter.

The first part of this chapter examines the reason for higher sampling rate needs in the SPWM multilevel converter. Having discovered that the higher sampling rate is an inherent requirement, the research examines next the technique of "phase shifting of the triangle carrier" applied to multiple modules of multilevel converters [35,36]. In the case of M = 8 modules, it has been found that K_c = 1 triangle carrier per modulating cycle suffices in synthesizing a very good voltage waveform. As the GTOs are pulsed only once per modulating cycle, the SPWM technique has the same switching loss as the Fundamental Frequency Method. This is the same switching rate as the 80 and 100 MVA size STATCOMS [26,25]. Simulation results also confirmed the linear amplifier property of SPWM as applied to multiple modules of multilevel converters with phase shifted carriers.

4.2 Requirement of High Frequency Triangle Carrier in Multilevel SPWM

Fig. 4.1 shows the schematic of a 3-phase, 5-level, diode clamped converter. The application of the SPWM strategy of one phase is illustrated in Fig. 4.2(a), which displays the sinusoidal modulating waveform against 4 bands of triangle carrier signals. Fig. 4.2(b) presents the switched waveforms at the ac terminal of the phase in question. Essentially, Fig. 4.2(b) is the superposition of the 2-level SPWM waveforms generated by the 4 bands of triangle carrier signals.

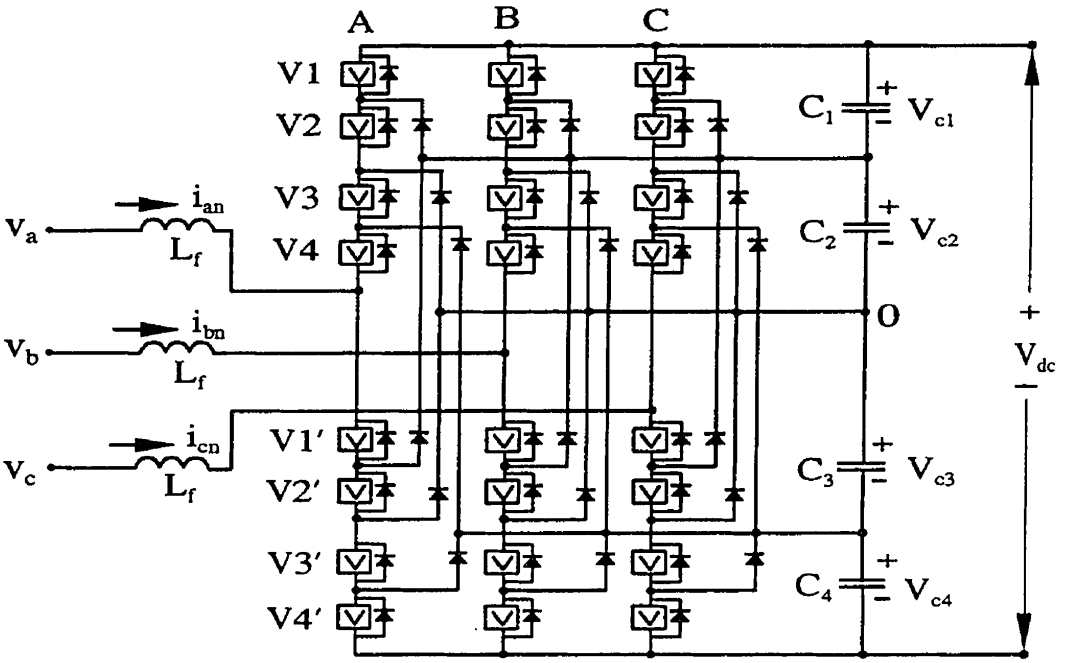


Fig. 4.1: Three phase diode-clamped 5-level converter.

4.2.1 Multilevel SPWM

The source of consternation is that K_c, the number of carrier triangles, has to be larger in a multilevel SPWM converter than in 2-level SPWM converter. The requirement for a higher triangle carrier frequency follows from the fact that at each level the

modulating signal is no longer the line-frequency sine-wave, but one of the 4 sliced sections $v_{i1}(t),..,v_{i4}(t)$ of the sine wave as illustrated in Fig. 4.3(a). The Fourier Series of the modulation waveform $v_i(t)$ in the j^{th} section is:

$$v_{ij}(t) = \sum_{K=1}^{K_m} A_{jK} \sin K\omega t + B_{jK} \cos K\omega t \qquad (4.1)$$

for j = 1,2,3,4; where A_{jK}, B_{jK} are the Fourier series coefficients of the k^{th} harmonic, $\omega = 2\pi/T$ the angular frequency for period T, and K_m is the maximum harmonic. The outputs of the SPWM strategy of each section are illustrated as $v_{o1}(t),..,v_{o4}(t)$ in Fig. 4.3(b).

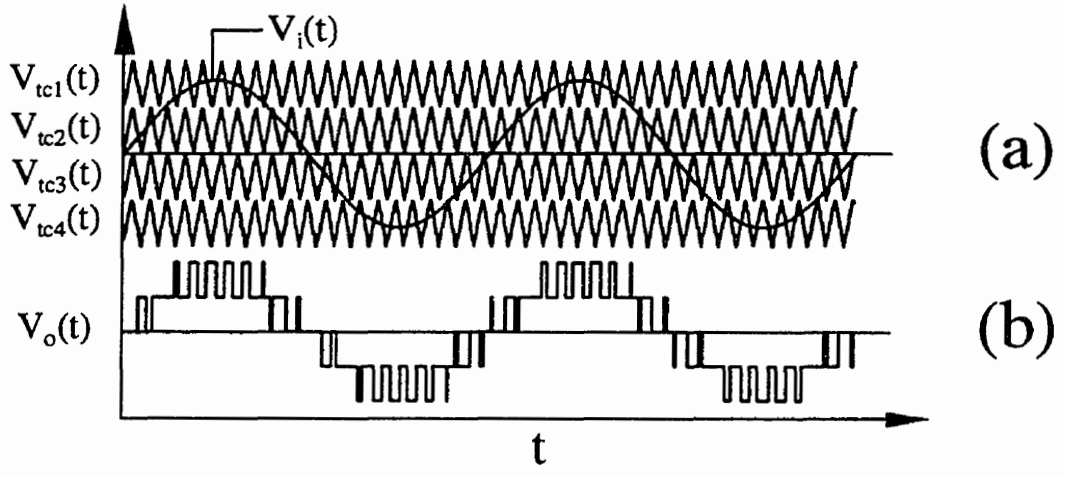


Fig. 4.2: SPWM technique applied to 5-level converter. (a) Modulating signal and triangle carriers. (b) 5-level output voltage.

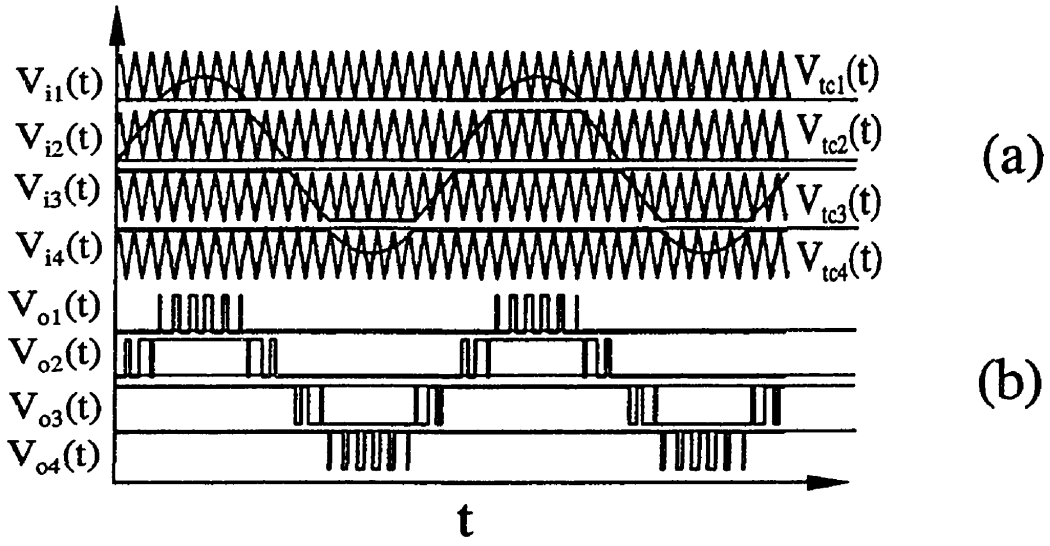


Fig. 4.3: SPWM strategy applied to each level. (a) Modulating signals and triangle carriers. (b) 2-level output voltages.

The Fourier spectra of the upper two sliced sections of the sine wave $v_{i1}(t)$, $v_{i2}(t)$ illustrated in Fig. 4.3(a) are shown in Fig. 4.4(a) and 4.5(a). One sees that the modulating signal of sliced sections occupy a bandwidth which is K_m multiples of ω. The Fourier spectra of the 4 sliced sections must reconstitute the original modulation sine-wave, that is

$$v_i(t) = \sum_{j=1}^{4} v_{ij}(t) = A\sin\omega t + B\cos\omega t \qquad (4.2)$$

It follows that the harmonics K = 2,3,..., K_m must be self cancelling that is:

$$\sum_{j=1}^{4} A_{jK} = 0 \qquad \sum_{j=1}^{4} B_{jK} = 0 \qquad (4.3)$$

for K = 2,3,..., K_m. The Fourier spectra of the lower two slices are identical to Fig. 4.4(a) and 4.5(a) but there is a 180° phase shift.

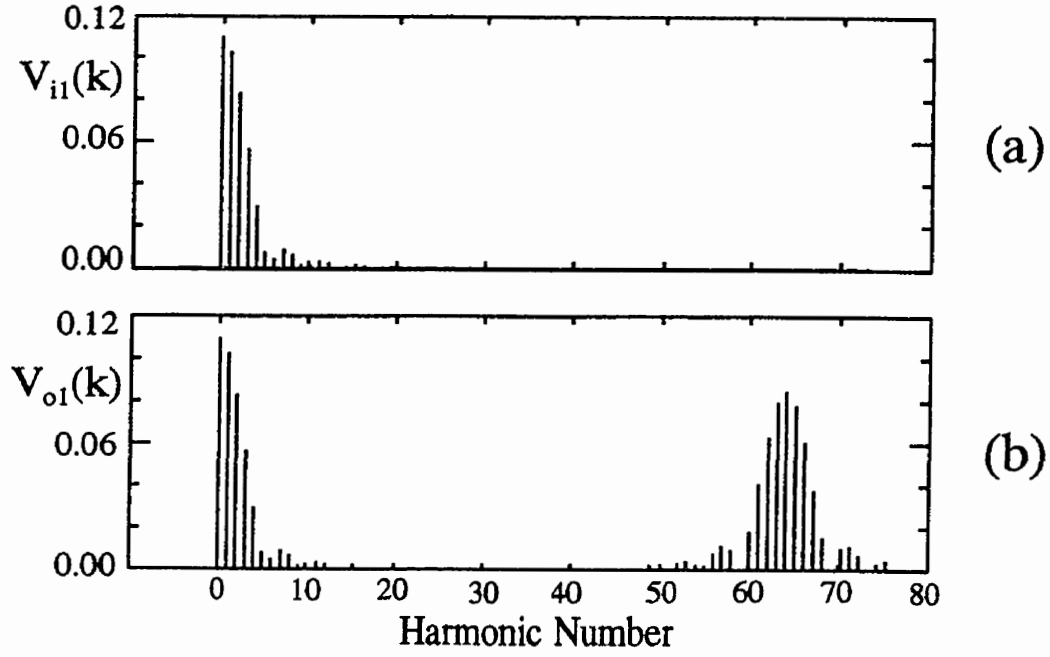


Fig. 4.4: (a) Fourier spectrum of $v_{i1}(t)$. (b) Fourier spectrum of $v_{o1}(t)$.

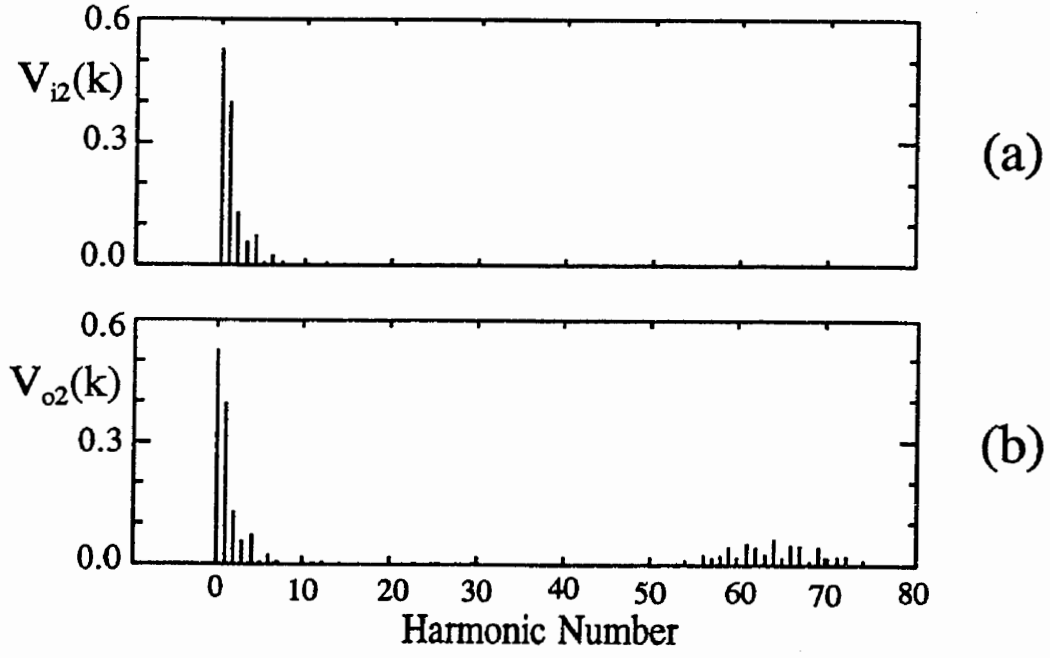


Fig. 4.5: (a) Fourier spectrum of $v_{i2}(t)$. (b) Fourier spectrum of $v_{o2}(t)$.

The SPWM technique is a linear amplification process. It can be proved mathematically [83] that the switched output waveform of the j^{th} section of Fig. 4.3(b) has the Fourier Series:

$$p_j(t) = G\left(\sum_{K=1}^{K_m} A_{jK} sinK\omega t + B_{jK} cosK\omega t\right) + n_j(t) \tag{4.4}$$

j = 1,2,3,4; where G is the gain and $n_j(t)$ is the switching noise, whose Fourier series is

$$n_j(t) = \sum_{K=K_N}^{\infty} D_{jK} sinK\omega t + E_{jK} cosK\omega t \tag{4.5}$$

j = 1,2,3,4.

Comparing (4.1) and (4.4), one observes that the input modulating signal is amplified by a constant gain G, with no phase shift. The summation of the pulsed outputs of all the levels is

$$v_o(t) = \sum_{j=1}^{4} p_j(t) \tag{4.6}$$

Substituting (4.4) and then (4.1) in (4.6)

$$v_o(t) = G\sum_{j=1}^{4} v_{ij}(t) + \sum_{j=1}^{4} n_j(t) \tag{4.7}$$

Finally, substituting (4.2) into (4.7)

$$v_o(t) = G(Asin\omega t + Bcos\omega t) + \sum_{j=1}^{4} n_j(t) \tag{4.8}$$

Thus the output contains the original input sinusoidal signal of (4.2), amplified by a constant gain G.

Fig. 4.4(b) and 4.5(b) show the Fourier spectra of the SPWM output pulses, $v_{o1}(t)$

and $v_{o2}(t)$, respectively. Fig. 4.6(a) and (b) show the spectra of the sum of the sliced inputs and outputs. Comparing Fig. 4.6(a) with 4.6(b) one sees that Fig. 4.6(b) contains the amplified spectrum of Fig. 4.6(a) together with the switching noise spectra of (5). The cancellation of the harmonics in (3) leaves the original amplified sine wave and the switching noise.

The fact that the bandwidth of the sliced sections of the sinewave of Fig. 4.4 extends to $K_m\omega$ requires the triangle carrier frequency $K_c\omega$ to be much higher than for the 2-level SPWM where the modulating frequency is only ω.

In the example of Fig. 4.4-4.6, it has been necessary to increase to $K_c = 63$ in order to achieve a THD of 5% for the 5-level converter.

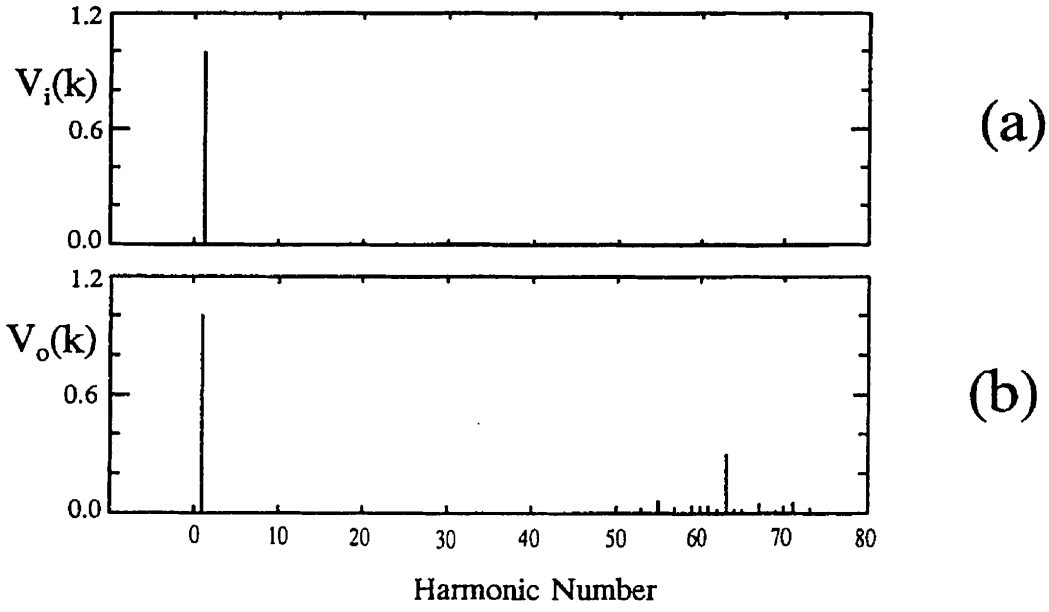


Fig. 4.6: (a) Sum of FFTs of input slices of the modulating signal. (b) Sum of FFTs of 2-level output voltages.

4.3 Operation of Multimodules of Multilevel Converters with Triangle Carrier Phase Shifting Technique

Unfortunately the switching loss of presently available GTOs is too large for such high switching frequency. One method of keeping the switching rate of the GTOs low is to use multiple converter modules whose GTOs are switched in staggered intervals to create the effect of a high sampling rate. In the method which comes under the name of "triangle carrier phase shifting technique" [35,36], the effective carrier triangles is K_{eff}, where $K_{eff} = MK_c$ and M is the number of converter modules.

The multimodular concept fits well in FACTS applications because the high MVA ratings require GTOs to be connected in series and/or in parallel in order to meet the high voltage and/or current ratings. This chapter extends the previous conceptual studies of parallel [36] and series [35] connected modules of 2-level SPWM converters to multilevel converters.

Fig. 4.7 depicts the multimodular converter based on parallel connections of M-modules of Fig. 4.1. In this chapter it is assumed that the dc voltages at the different levels are all equal, that is: $V_{c1} = V_{c2} = V_{c3} = V_{c4}$.

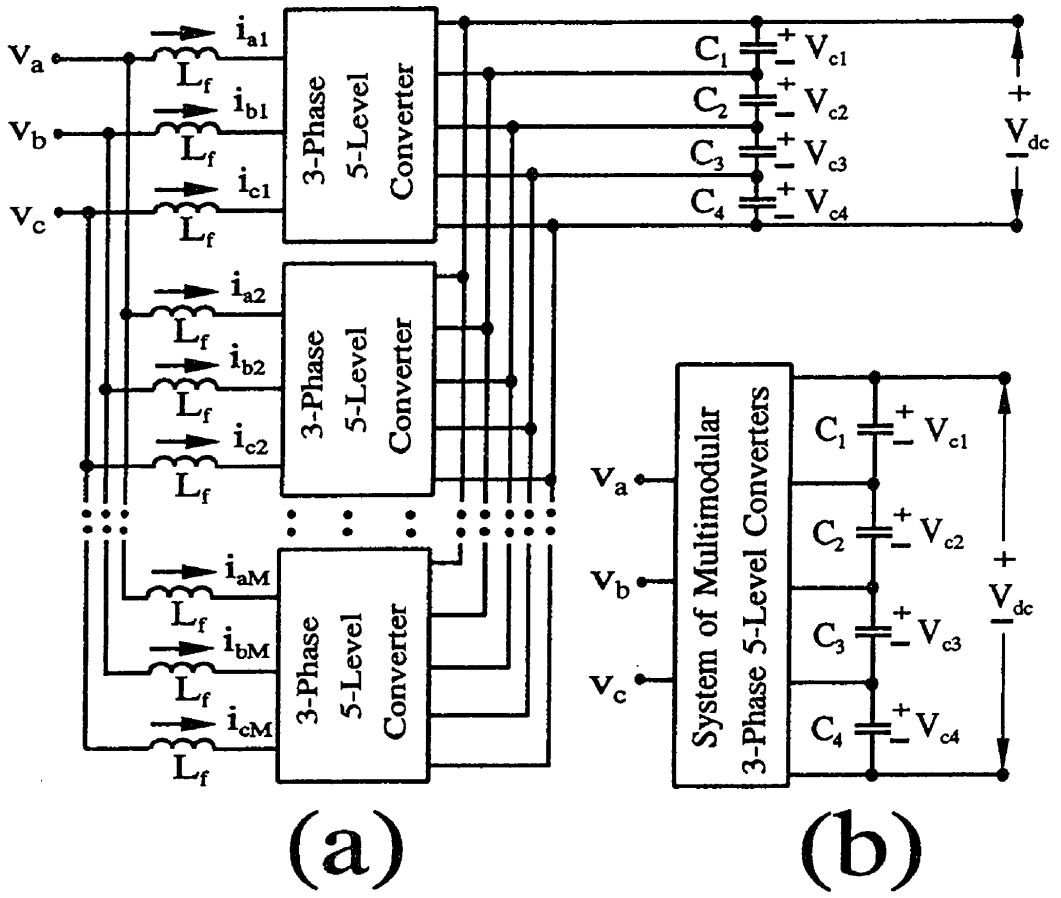


Fig. 4.7: System of multimodular 3-phase 5-level converters. (a) schematic (b) symbol.

4.3.1 SPWM Strategy

The switchings of the GTOs in each module m = 1, 2,..., M are determined by the multilevel SPWM strategy of Fig. 4.2. The same 3-phase sinusoidal modulating waveforms are received by the switching logic controller of each converter.

4.3.2 Phase Shifted Triangle Carriers

The switching logic controller of each module, however, receives its unique

triangle carrier which is phase-shifted with respect to its neighbours. As illustrated in Fig. 4.8, the modulating period 2π, is divided by K_c triangles so that the period of the triangle carrier is $\theta_c = 2\pi/K_c$. The triangle phase shift for M modules is $\theta_{sh} = \theta_c /M$. Fig. 4.8 shows the phase shifted carriers of modules m = 1, 2, and 8, with M = 8.

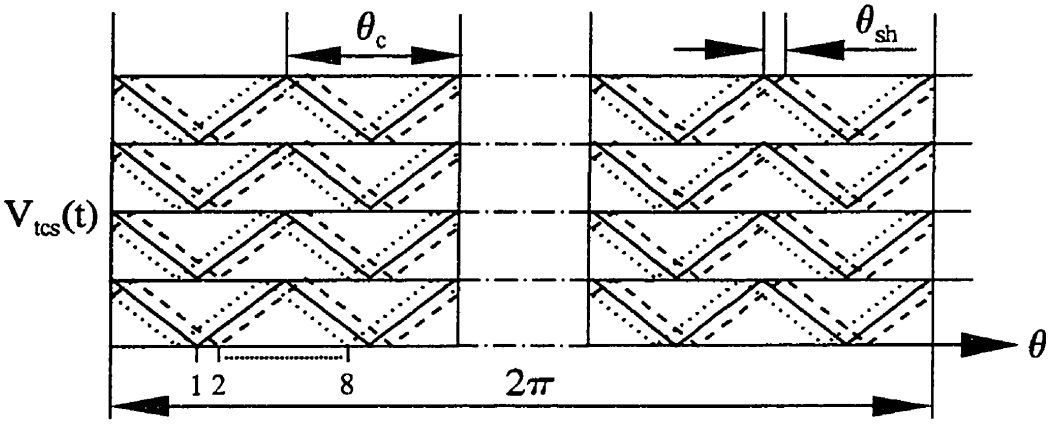


Fig. 4.8: Equally phase shifted triangle carriers for m = 1, 2, 8 in 8 modules of 3-phase 5-level converter system.

4.3.3 Minimum Switching Loss SPWM

A very desirable finding in the research is that operation with $K_c = 1$ is feasible. The GTOs are pulsed only once per cycle so that the switching loss is minimum. Fig. 4.9(a) illustrates the sinusoidal modulating signal and 3 phase shifted triangle carrier waveforms of the 4 bands. Fig. 4.9(b) show the voltage output waveforms V_{o1}, V_{o2},..., V_{o8} of the 8 modules. Fig. 4.9(c) shows the equivalent output voltage which is formed by the average of V_{om}, m = 1,2,..,8. It shows a very good approximation of the modulating sine wave. FFT measurement shows that its THD is 3.5% or less for modulation index variation between 95% and 105%.

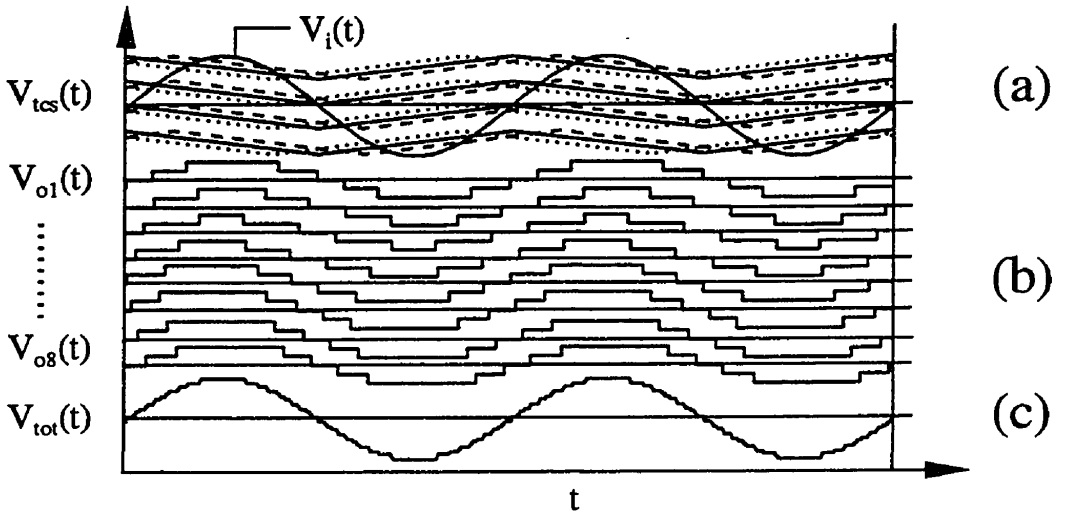


Fig. 4.9: (a) Sinusoidal input modulating signal with phase shifted triangle carriers (b) Outputs for single converters (c) Average output for 8 modules.

4.3.4 Input/Output Linearity

An important property of the SPWM strategy is the ease of controlling the output voltage by electronically controlling the modulating signal. Thus by varying the amplitude of modulating sinusoidal waveform, in Fig. 4.9(a), one varies the amplitude of the output voltage in Fig. 4.9(c).

Fig. 4.10 plots the fundamental harmonic component of the output voltage against the modulation index. One sees another desirable property in SPWM, namely linearity between the output voltage magnitude and the modulation index.

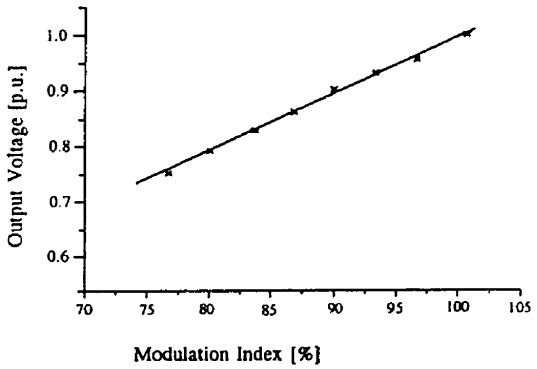


Fig. 4.10: Linearity with respect to modulation index.

Linearity, as implied by the description of linear amplifier is demonstrated in Fig. 4.11 and 4.12. In Fig. 4.11(a), the modulating signal contains a 12.5% third harmonic. The output voltage in Fig. 4.11(c) reproduces the input signal. Fig. 4.12 contains the FFT analysis of Fig. 4.11(c) showing the fundamental and 12.5% third harmonic. The 12.5% third harmonic flattens the modulating signal so that the modulating index of the fundamental frequency can be increased to 1.15 pu. The linear amplifier property is valuable because when inputs of arbitrary waveforms can be amplified with a constant gain without delay, the inputs can include feedback control signals and active filtering signals.

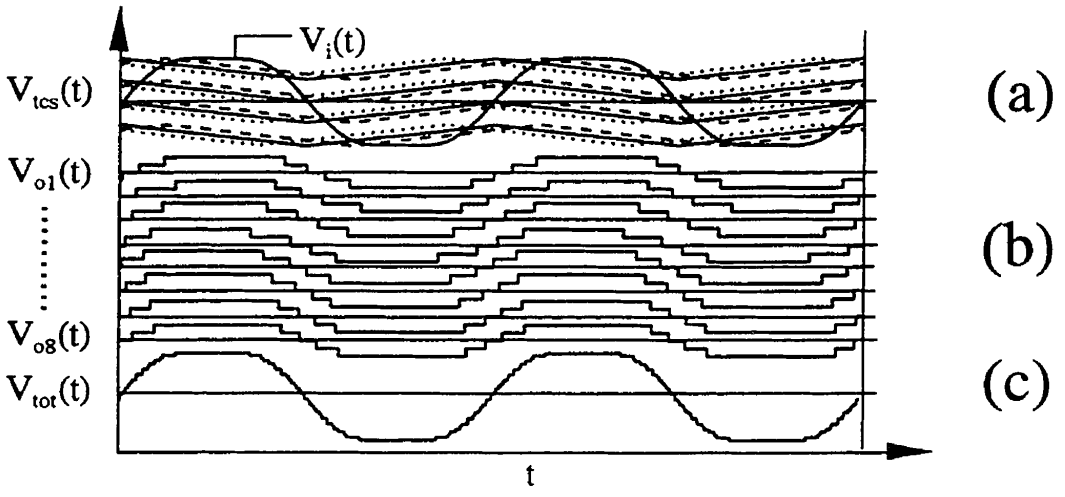


Fig. 4.11: (a) Band limited modulating signal with phase shifted triangle carriers (b) Output of single converters. (c) Average output for 8 converters.

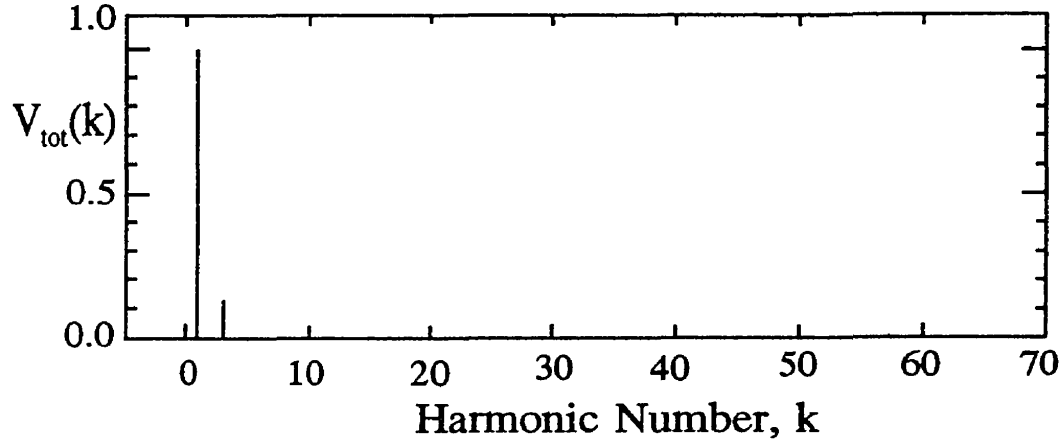


Fig. 4.12: Fourier spectrum of Fig. 4.11(c).

4.4 Total Harmonic Distortion (THD) of Voltage

Fig. 4.13 and 4.14 are results on achievable THD of voltage plotted against modulation index which have been compiled from extensive simulations. In Fig. 4.13, the number of converters is 8 and the objective is to study the effect of increasing the number of the levels. In Fig. 4.14, the levels are fixed at 5 and the objective is to study the effect of increasing the number of converters.

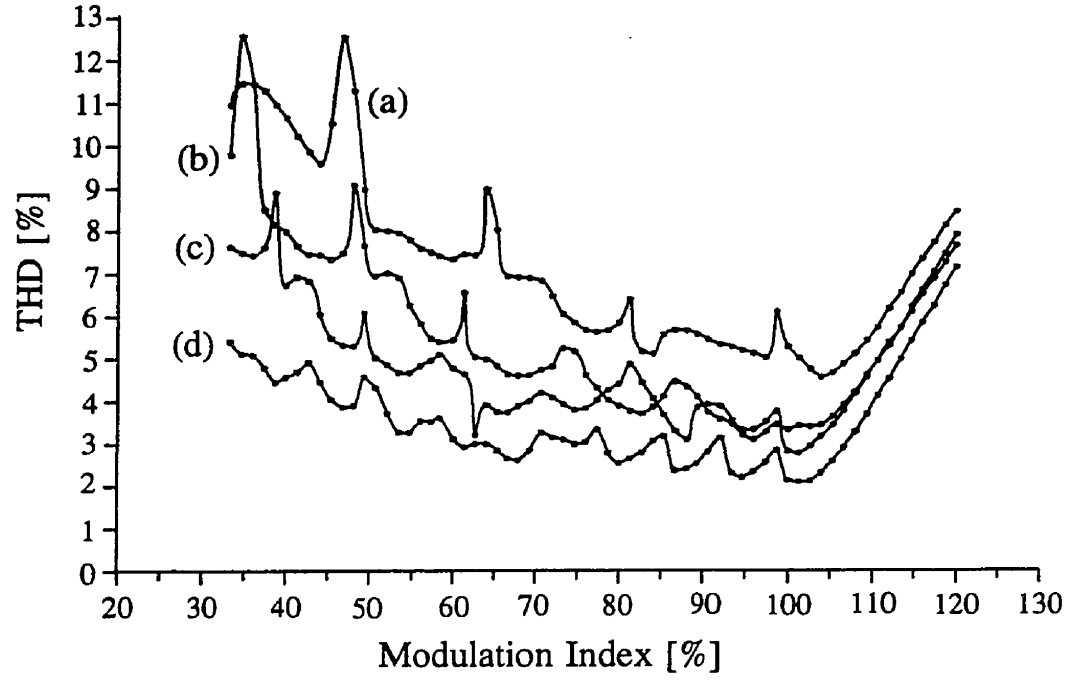


Fig. 4.13: Variation of THD of voltage with respect to modulation index for 8 modules. (a) 4-level (b) 5-level (c) 6-level (d) 8-level.

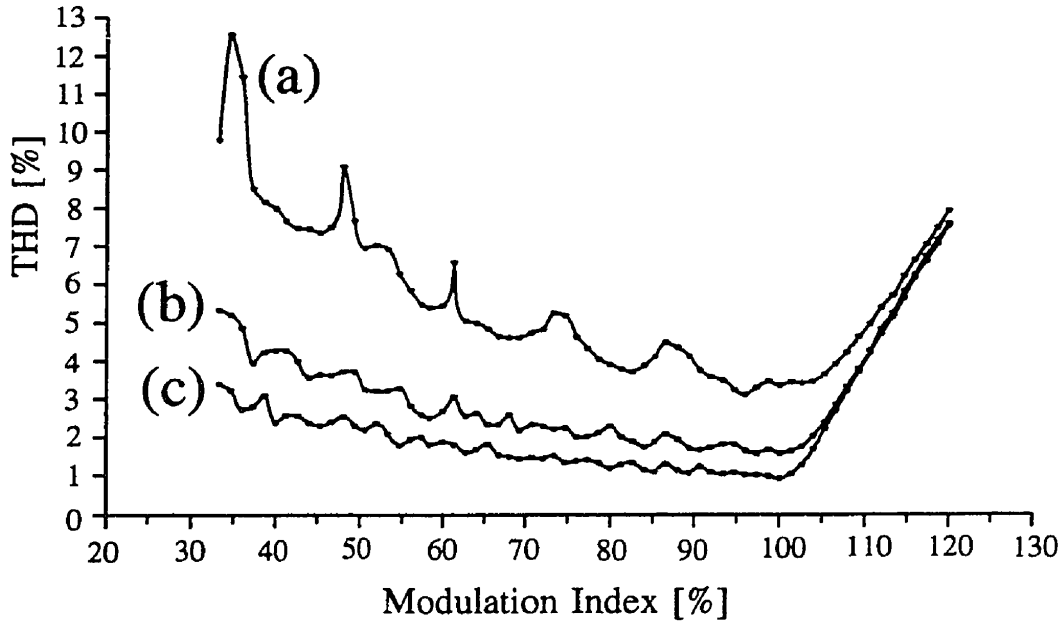


Fig. 4.14: Variation of THD of voltage with respect to modulation index for multimodular 5-level converters. (a) 8 modules (b) 16 modules (d) 24 modules.

4.5 Regulation and Equalization of dc Voltages

Critical to the operation of the multimodular multilevel system of Fig. 4.7 is the ability to regulate V_{dc} and to equalize V_{cj} (j=1,2, .. 4) by feedback controls. Fig. 4.15 is the proposal for the multimodular system. In the outer feedback loop, the error $\epsilon = V_{REF} - V_{dc}$ after passing through the proportion-integral (PI) block is applied to shift the phase angle of the modulating signal $V_i(t)$ of Fig. 4.10(a) so as to admit or invert real ac power so as to null the error.

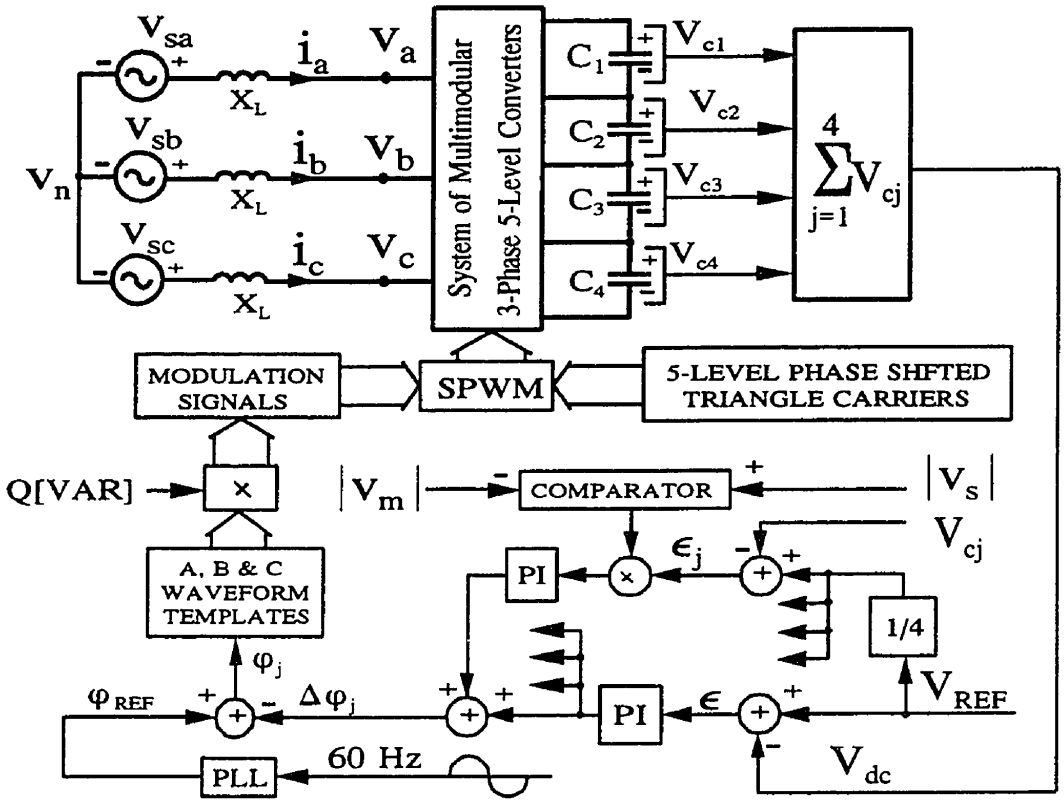


Fig. 4.15: Proposed scheme for regulation of dc voltage and equalization of capacitor voltages under shunt SVC operation.

The inner feedback loops use the error ϵ_j of the j^{th} capacitor voltage to advance

or retard the angle of the j^{th} portion of the modulating signal corresponding to the j^{th} capacitor, with respect to the angle already set by the outer feedback loop. This has the effect of adjusting the real power admitted or inverted in the j^{th} capacitor until the error ϵ_j is nulled.

Experiences from both [82] and this research have shown that the feedback loops are highly non-linear and finding the correct proportional and integral constants for stabilization is still an art. The task is made easier by large capacitors. An alternative fall-back technology available is the use of chopper circuits for equalization [84].

4.6 Active Filtering

As the SPWM strategy enables the multiple modules of multilevel converters to process the modulating signals as three high power linear amplifiers, active filtering of power system harmonics can be implemented through it. Fig. 4.16 and 4.17 show simulation results to illustrate the action of active filtering. Firstly in Fig. 4.16, a 5^{th} harmonic noise is introduced to the source voltage V_s shown in Fig. 4.16(d). The multimodule multilevel array is operated as a shunt-STATCOM. As the modulating signal is a sine wave as shown in Fig. 4.16(a), the total output voltage is its linearly amplified form as shown in Fig. 4.16(c). The line current in Fig. 4.16(d) contains a large fundamental component (which is determined by V_{tot} and the fundamental component in V_s) and a 5^{th} harmonic component (from the 5^{th} harmonic component in V_s).

In order to eliminate the 5^{th} harmonic component, the STATCOM must produce a 5^{th} harmonic voltage which is equal in magnitude but opposite in time phase from that in V_s. The simulated current, i_s, in Fig. 4.17(d) shows that this is achieved in the

The active filtering algorithm must be able to produce this equal and opposite 5th harmonic in the total output voltage in the STATCOM as shown in Fig. 4.17(c) and tracing it to the source, the 5th harmonic must ride on the modulating signal as shown in Fig. 17(a).

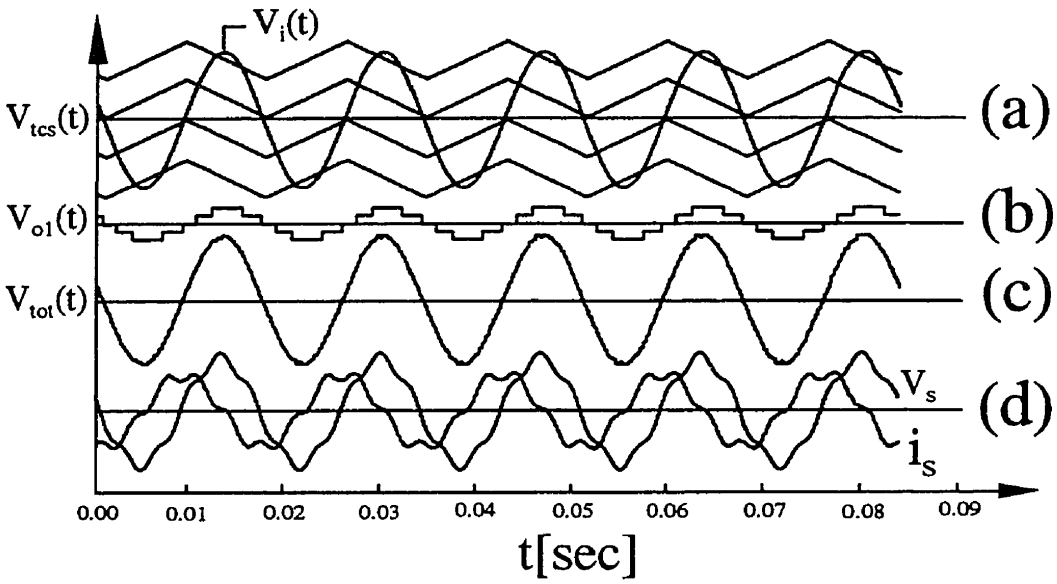


Fig. 4.16: Operation as shunt-STATCOM when active filtering is disabled. (a) Modulating input signal and 1 set of triangle carriers. (b) Output voltage for single module. (c) Total average output voltage for 8 modules. (d) Source voltage, V_s, and current, i_s.

The research in active filtering consists of finding feedback methods which add the appropriate modulating signal which will null the noise voltage from V_s. The high-power, high-gain linear amplifier capability is essential to bridge the microwatt signal level in Fig. 4.17(a) to the hundreds of kV output in Fig. 17(c).

The active filtering algorithm is based on using negative feedback with the very large gain to attenuate the 5th harmonic. The notch filter tuned to the fundamental

frequency is placed in the feedback loop so that the line current at fundamental frequency is attenuated.

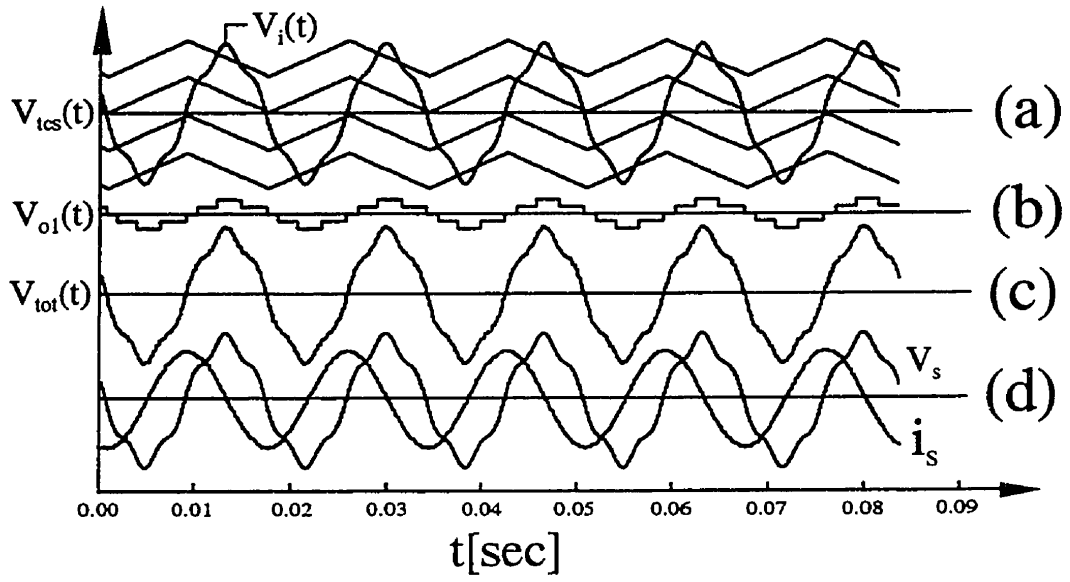


Fig. 4.17: Operation as shunt-STATCOM when active filtering is enabled. (a) Modulating input signal and 1 set of triangle carriers. (b) Output voltage for single module. (c) Total average output voltage for 8 modules. (d) Source voltage, V_s, and current, i_s.

4.7 Summary

In this chapter, it has been shown that the SPWM strategy, as applied to multilevel converters, inherently requires a higher triangle carrier frequency than in application to the 2-level converter. In order to keep the switching loss low, the "phase shifting triangle carrier technique" of [35,36] is applied to multimodules of multilevel converters because the effective carrier triangular number is increased by the multiple of the number of modules. A surprising and attractive finding of this research is that it is possible to obtain THD = 3.5% when modules are operated with the GTOs switching at 1 pulse per

modulating frequency cycle, which is the same rate employed in the existing installations of STATCOMS [25,26].

Tests establish that the output/input relationship is linear and as low a voltage THD as desired can be obtained by increasing the number of modules and/or the number of levels in the converters. Furthermore, the simulation test results have shown that the system of multiple modules of multilevel converters under SPWM strategy can be employed to perform active filtering.

More research is required to prove that such a multimodular multilevel converter station can be realized economically. Of particular importance, the GTOs must share the current loadings equally. More research is also required to establish a theory for operation.

CHAPTER V

DIODE-CLAMPED MULTILEVEL CONVERTERS AS SERIES-STATCOM

5.1 Introduction

The previous chapter has successfully provided explanations as to why the sinusoidal pulse width modulation (SPWM) strategy requires a higher carrier frequency in the multilevel converter than in the 2-level converter. Furthermore, if the SPWM strategy must be applied, then multimodules of multilevel converters operated by the phase-shifted triangle carrier technique yield excellent waveforms even for the switching rate of 1 pulse per modulating cycle.

In this chapter, the research turns from the research of the modulation method of chapter III to experimental research in applications. As the modulation method is not an issue in application, the multilevel converter is controlled by the fundamental frequency method of switching in this chapter. In addition to the tests of the multilevel converter applied as a series-STATCOM, which will be described in subsequent sections, the laboratory research program gives experimental validation to:

(1) the feedback strategy of the dc voltage regulation loop [42,82,85].

(2) the feedback strategy of the individual capacitor voltage equalization loops [42,82,85].

(3) the real-time digital control by the TMS320-C40 DSPs and FPGA.

There are presently several publications on the applications of the diode-clamped multilevel converter as shunt-STATCOMs [40,41,44,54,63,64,81,82,85], but none on the series-STATCOM.

In many aspects, the series-STATCOMs and the shunt-STATCOMs are similar. For this reason, the results presented here emphasize the aspects in which the requirements of the series-STATCOM are different from those of shunt-STATCOM. Firstly, in order to implement series compensation in the radial transmission line, transformers are required to provide galvanic isolation from the lines so that the three legs of the multilevel converter can be connected to common dc links. Secondly, it is the practice of transmission line engineering to allow the zero sequence currents to flow during faults, so that it is necessary to connect the secondary windings of the 3-phase transformers in delta so that the zero sequence secondary currents have a path as the circulating current of the delta. Thirdly, as a series controller, in the event of a single-line or two-line outages (brought about by the opening of circuit breakers during short circuit faults), the converter must continue to provide compensation to the surviving line(s). Fourthly, the series-STATCOM must be capable of turning-OFF safely while transmitting the full power. Fifthly, the series-STATCOM, following the turn-OFF, must be capable of recovering control. Because of the experimental facility, it is possible to establish that the multilevel series-STATCOM can cope with all these requirements affirmatively.

5.2 Model of Radial Transmission Line in Series-STATCOM Studies

Fig. 5.1(a) shows a radial transmission line modelled as a line reactance jX_L between the sending-end voltage $\mathbf{V}_s$ and the receiving-end voltage $\mathbf{V}_r$. The series-STATCOM is modelled as an ac reactance voltage source $\mathbf{V}_c$. Fig. 5.1(b) shows the phasor diagram of the voltages and current. The reactance voltages, $jX_L\mathbf{I}$ and $\mathbf{V}_c$, are perpendicular to the current phasor, I. As can be seen, the function of the voltage $\mathbf{V}_c$ of

the series-STATCOM is to compensate the large inductive reactance drop jX_LI, so that large real ac power $P=V_sI\cos(\delta_{sr}/2)$ can be sent through the line in spite of the large line inductive reactance jX_L. By varying the magnitude of V_c, the series-STATCOM also acts as a controller of the amount of real ac power transmitted.

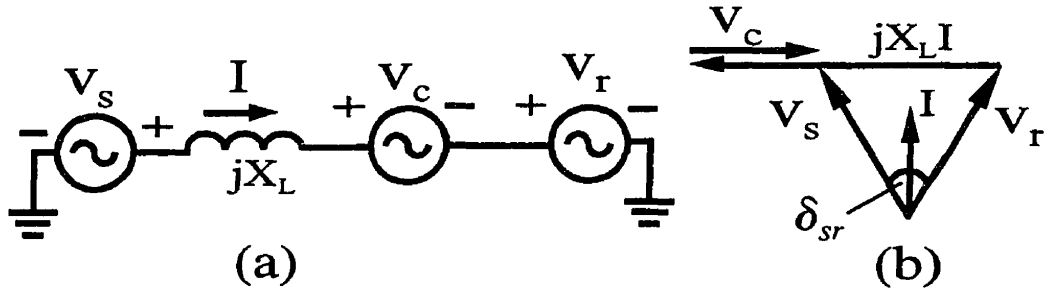


Fig. 5.1: Single-line diagram of transmission system.

5.3 Experimental Set-up of Laboratory Tests

For the purpose of the tests in the experimental research, the sending-end and the receiving-end voltages can be combined as $V_{sr}=V_s-V_r$, with the circuit representation of Fig. 5.2(a). As the resistances in the laboratory components are not negligible, the representation of its voltage **RI** is included in the phasor diagram of Fig. 5.2(b). When the level of compensation by the series-STATCOM approaches 100%, the voltage angle, δ_{sr} is small, and V_{sr} has only a small magnitude.

Fig. 5.3 shows the block diagram of the test components: the three-phase, 60 Hz voltage source V_{sr}, the transmission line inductive reactance jX_L and the 6-level STATCOM, connected by way of transformers, which require some explanation here.

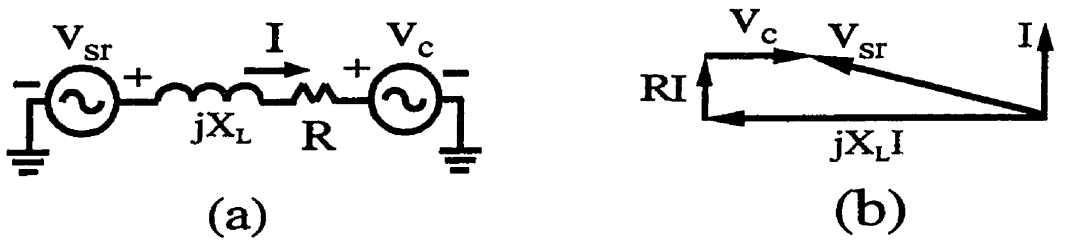


Fig. 5.2: Series capacitor compensation.

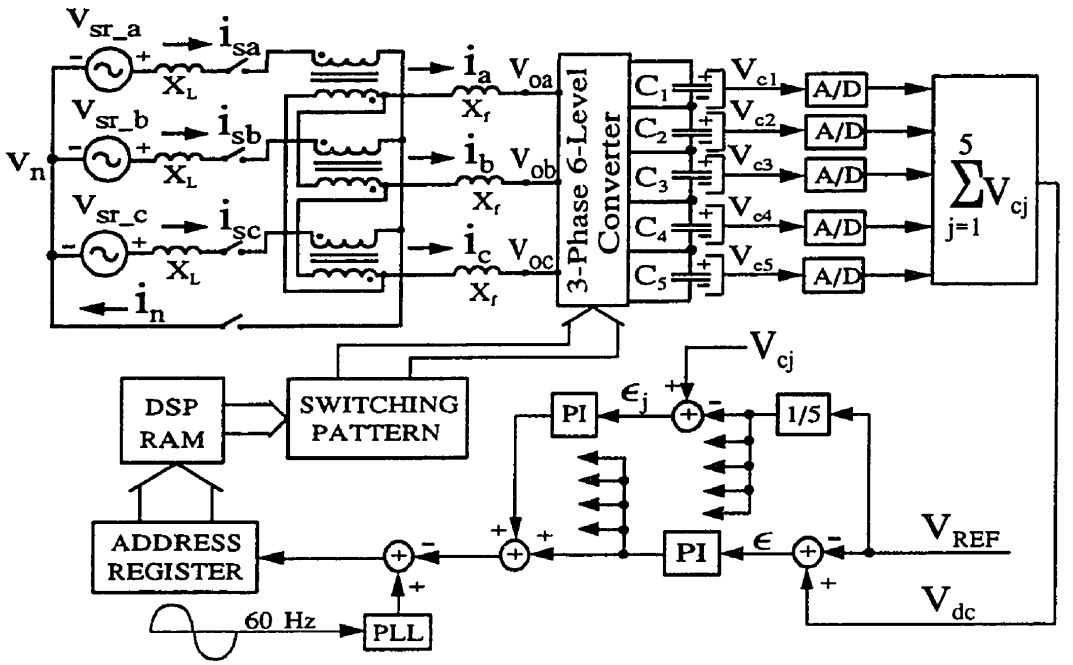


Fig. 5.3: Block diagram of the experimental setup.

In the field, the primary windings of the transformers are inserted in series with transmission lines, so that they "float" with the voltages of each phase of the transmission lines. During faults, the zero-sequence currents pass from the grounded neutral-point of the star connected sending-end voltages V_s, through the transmission lines and the transformer primary windings to the grounded neutral-point of the star-connected

receiving-end voltage V_r, taking a return path through the ground. This is modeled in Fig. 5.3 by a fourth line joining the neutral points of the star connected V_{sr} and transformer primaries. The transformer secondaries are delta connected so that the zero sequence currents have the delta loop as the path to circulate. The 4 knife switches provide the means to study line outages.

Fig. 5.3 also shows the control blocks of the 6-level converter. A full description of their functions is given in [63,82,85]. It needs only to mention that the outer feedback loop regulates the dc voltage and in the process ensures the condition of reactance voltages at the ac terminals. Five inner feedback loops equalize the dc capacitor voltages between the 6 levels.

5.4 6-Level Converter

Some words of explanation are required concerning the choice of the 6-level converter of Fig. 5.4 in the program of tests. As mentioned previously, the available laboratory facilities are in the forms of 3-phase, voltage-source bridge converter modules, and it is a matter of necessity to adapt them for multi-level converter research. At the off-set, it needs to be stated that Fig. 5.4 is not suitable for FACTS application, as the dc capacitor voltage across each level does not "protect" the solid-state switches from high voltages as in the case of the 6-level, "diode-clamped circuitry" of Fig. 5.5, which is the appropriate circuit for high voltage application. However, as the principles, regarding the charging of the capacitors at the many levels and the operation as a STATCOM, are similar, the experimental test results of the 6-level converter of Fig. 5.4 have validity for the diode-clamped topology of Fig. 5.5. This view is supported by the comparable digital

simulation results of STATCOMs based on Fig. 5.4 and Fig. 5.5.

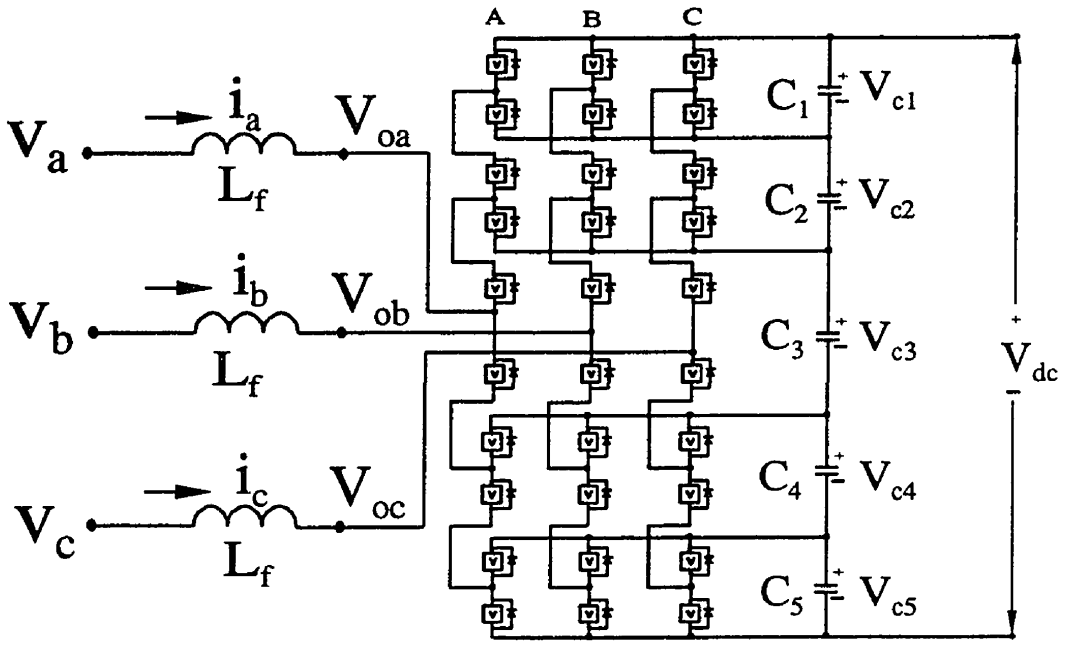


Fig. 5.4: Schematic of laboratory 6-level converter.

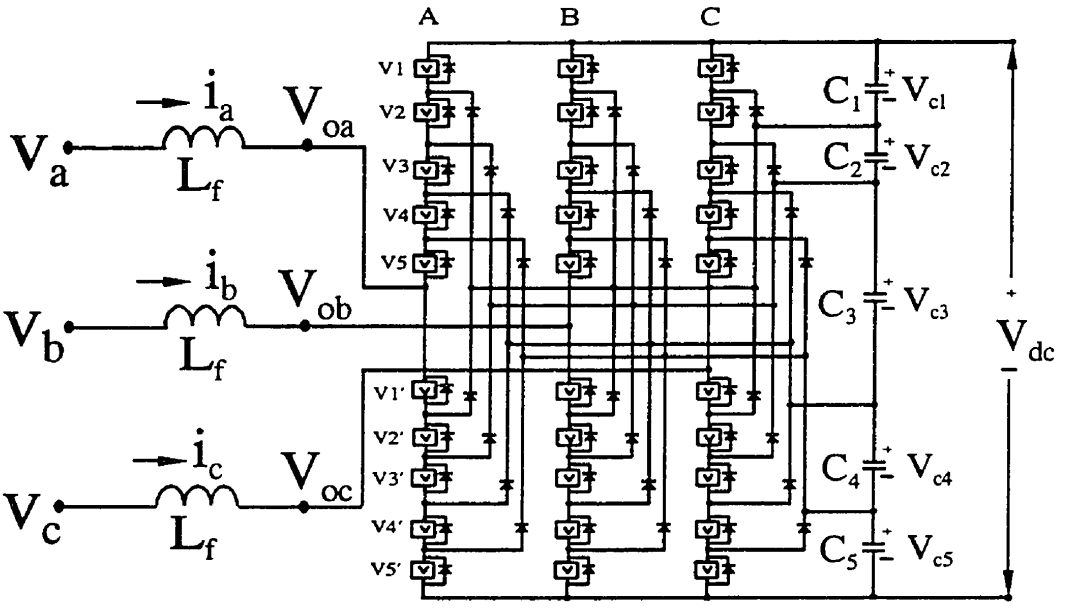


Fig. 5.5: Schematic of diode-clamped 6-level converter for STATCOM application.

5.5 Test results: Balanced 3-phase Operation as Series-STATCOM

Fig. 5.6 shows in (a) the phase-to-midpoint voltage, and (b) the line-to-line voltage of the 6-level converter. Fig. 5.7 shows in (a) the current leading the voltage by 90 degrees and in (b) the balanced three phase currents, thus demonstrating that the capacitive reactance operating condition of the series-STATCOM has been successfully implemented by the outer dc voltage regulation feedback loop. The currents owe their excellent waveforms to three factors: (i) the fundamental frequency switching strategy which eliminates the 5^{th} and 7^{th} harmonics, (ii) the inner feedback loops which equalize the dc capacitor voltages and (iii) the large line inductive reactance. As the 6-level converter has only 2 degrees of freedom in the design of the switching angles and these have been committed to the elimination of the 5^{th} and 7^{th} harmonic, ac voltage magnitude is controlled through the setting of the dc link voltage reference, V_{REF} in Fig. 5.3.

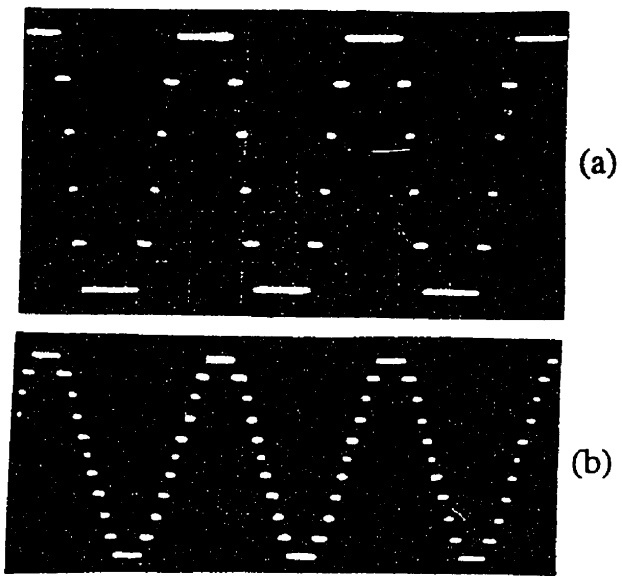


Fig. 5.6: Output voltages of the 6-level converter. (a) phase-to-midpoint (V_{oa}) (b) line-to-line (V_{oa}-V_{ob})

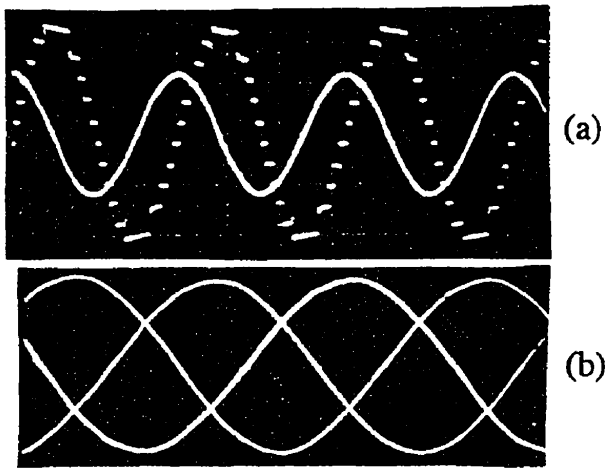


Fig. 5.7: Operation under balanced 3-phase. (a) phase voltage and phase current on the converter side. (b) 3-phase line currents on the line side.

5.6 Test Results: Line Outages

Unlike a shunt device, the series-STATCOM must continue to provide continuity of current flow through the remaining intact line(s) in the event of single-line or two-line outages. These outages occur following short circuit faults which cause the line circuit breakers to open so as to isolate the faults. The survivability of the multi-level converter is easily demonstrated in the experimental set-up by opening the knife switches of the C-line or both the B- and C-lines while operating under load.

5.6.1 Two-lines Outage with Neutral Return Closed

When both the B- and C-knife switches are open, the oscillogram in Fig. 5.8 shows the surviving line current, i_{sa}, and its return as the neutral current, i_n, on the primary-side. In order to understand the situation, the circuit of Fig. 5.3 is redrawn as Fig. 5.9. The multi-level converter is represented by ideal voltage sources $\mathbf{V}_{ab}$, $\mathbf{V}_{bc}$ and

V_{ca} the line-to-line voltages of the converter inputs. Fig. 5.9 displays the pattern of current flow $i_n=-i_{sa}$, $i_b=-i_a$. The secondary current i_x takes a path through the converter voltage V_{ab}. The oscillogram in Fig. 5.10 shows the transformer secondary-side current i_x, leading V_{ab} the converter voltage by 90 degrees. It is clear that the 6-level converter continues to operate as a series STATCOM in spite of the outages in the other 2 lines. The dc voltage regulation feedback loop and the equalization feedback loops maintain the dc voltage levels from the surviving line current so that the voltage waveform does not differ from that of the balanced operation in Fig. 5.6 and Fig. 5.7.

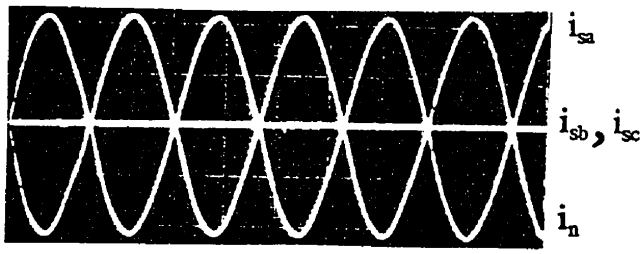


Fig. 5.8: Fault conditions on the line side. B and C phases open with neutral closed. Current waveforms on the line side.

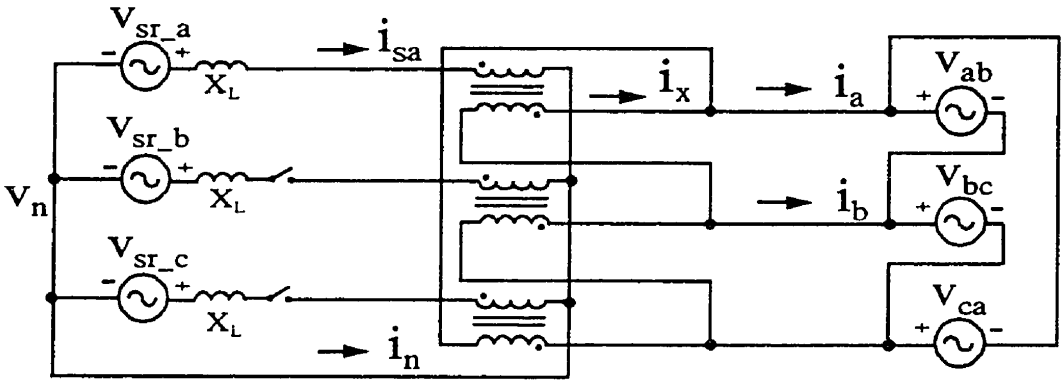


Fig. 5.9: Fault conditions on the line side. B and C phases open with neutral closed.

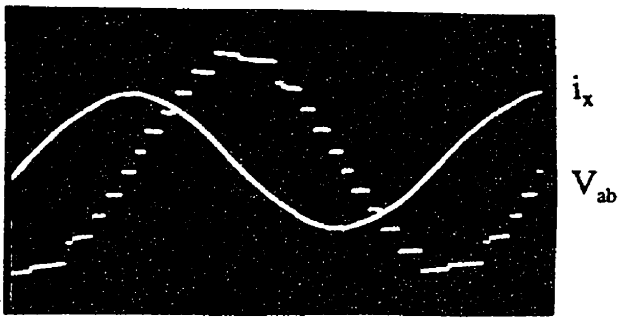


Fig. 5.10: Fault conditions on the line side. B and C phases open with neutral closed. Voltage and current waveforms on the converter side.

5.6.2 Single-Line Outage with Neutral Return Closed

When only the C-knife switch is open, the oscillogram in Fig. 5.11 shows the surviving line currents i_{sa} and i_{sb} and their return as the neutral current ($-i_n=i_{sa}+i_{sb}$). The line currents i_{sa} and i_{sb} are 120 degrees apart and both share the same return path through the ground (fourth) line.

This situation can be viewed as the superposition of two cases: firstly with B- and C-lines open as in the previous section and secondly, with A- and C-lines open. For the second case when the A- and C-lines are open, Fig. 5.12 shows the pattern of flow of the surviving current, $i_{sb}=-i_n$ and i_y, in the primary and secondary sides of the b-transformer. The current i_y has a return path as i_b and $-i_c$ through $\mathbf{V}_{bc}$.

The case of the outage of the C-line alone consists of the superposition of Fig. 5.9 and 12. Thus the line current $-i_n=i_{sa}+i_{sb}$. In fact, the oscillograms of the transformer secondary-side current i_x and the converter voltage $\mathbf{V}_{ab}$ and that of the current i_y and the converter line-to-line voltage $\mathbf{V}_{bc}$ are both similar to Fig. 5.10 and for this reason are not reproduced here.

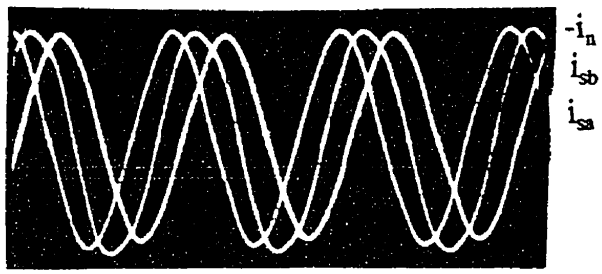


Fig. 5.11: Fault conditions on the line side. C phase open with neutral closed. Current waveforms on the line side.

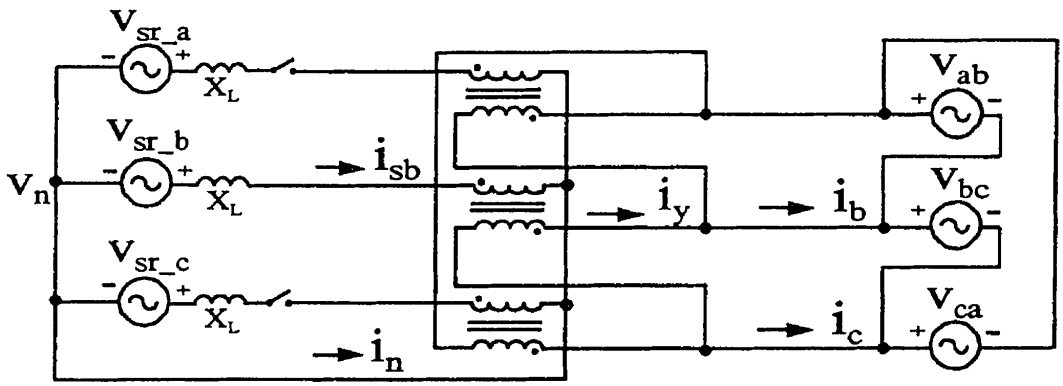


Fig. 5.12: Fault conditions on the line side. A and C phases open with neutral closed.

5.6.3 Single Line Outage with Neutral Return Open

The oscillogram of Fig. 5.13 is for the same outage in the C-line but with the knife switch in the ground return line open. As i_{sb} must be the return of i_{sa}, the phase angle between them is 180 degrees and not 120 degrees as in Fig. 5.11. The simultaneous occurrence of the single-line outage with an accidental severance of the neutral line is rare, but this possibility cannot be ruled out. The STATCOM is robust enough to withstand this severe fault.

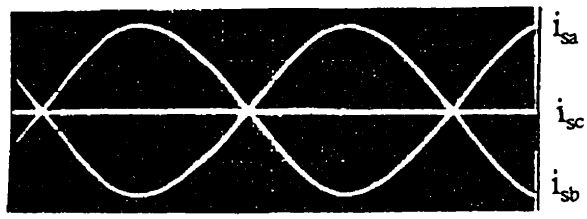


Fig. 5.13: Fault conditions on the line side. C phase open, with neutral open. Current waveforms on the line side.

As part of the fundamental research, investigation has been carried out as to how the converter accommodates this situation. Fig. 5.14 shows the pattern of the flow of the primary and secondary currents. Since $i_{sb}=-i_{sa}$, it is sufficient to describe all secondary currents in terms of the phasor $\mathbf{I}_a=\mathbf{I}_x$ of the a-transformer secondary current. Therefore, $\mathbf{I}_x=\mathbf{I}_a$, $\mathbf{I}_y=-\mathbf{I}_a$, $\mathbf{I}_z=0$, and $\mathbf{I}_b=-2\mathbf{I}_a$, $\mathbf{I}_c=\mathbf{I}_a$. The current flowing through $\mathbf{V}_{ab}$, $\mathbf{V}_{bc}$ and $\mathbf{V}_{ca}$ are $\mathbf{I}_x=\mathbf{I}_a$, $\mathbf{I}_y=-\mathbf{I}_a$ and $\mathbf{I}_z=0$ respectively.

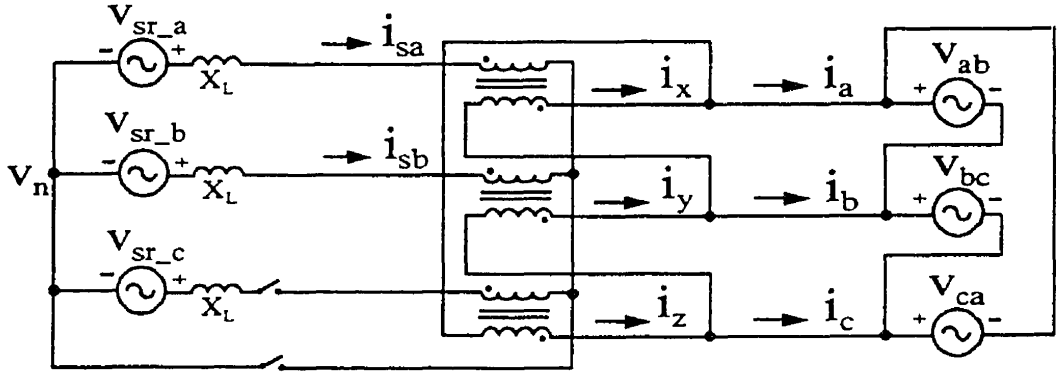


Fig. 5.14: Fault conditions on the line side. C phase open with neutral open.

The dc voltage regulation feedback loop must rotate the voltage phasors $\mathbf{V}_{ab}$, $\mathbf{V}_{bc}$ and $\mathbf{V}_{ca}$ with respect to $\mathbf{I}_a$ until it finds an equilibrium position in which the ac power is

converted to zero dc power. Fig. 5.15 shows such an alignment of the converter voltages $\mathbf{V}_{ab}$, $\mathbf{V}_{bc}$ and $\mathbf{V}_{ca}$ with respect to the

current $\mathbf{I}_a$. The requirement

$$Real(V_{ab}I_x^* + V_{bc}I_y^*) = Real(V_{ab}I_x^* - V_{bc}I_x^*) = 0 \qquad (5.1)$$

is satisfied in Fig. 5.15 where $\mathbf{I}_x=\mathbf{I}_a$ leads $\mathbf{V}_{ab}$ by 120 degrees and confirmed by the oscillogram of Fig. 5.16(a), and $\mathbf{I}_y=-\mathbf{I}_a$ leads $\mathbf{V}_{bc}$ by 60 degrees as shown in the oscillogram of Fig. 5.16(b). The voltage $\mathbf{V}_{ab}$ rectifies as much ac power as is inverted by the voltage $\mathbf{V}_{bc}$.

Further experimental confirmation is found in the oscillograms of Fig. 5.17(a), (b) and (c) which show the current and voltage pairs ($\mathbf{I}_a$, $\mathbf{V}_{ab}$), ($\mathbf{I}_b$, $\mathbf{V}_{bc}$) and ($\mathbf{I}_c$, $\mathbf{V}_{ca}$) respectively. The magnitudes of the currents in Fig. 5.17(a), (b) and (c) are proportional to $\mathbf{I}_a=\mathbf{I}_a$, $\mathbf{I}_b=-2\mathbf{I}_a$ and $\mathbf{I}_c=\mathbf{I}_a$. The currents in (a), (b) and (c) are 120 degrees leading, 60 degrees leading, and in phase with respect to the voltages.

On the primary side, the STATCOM voltage across the a-b phases is proportional to $\mathbf{V}_{ab}$-$\mathbf{V}_{bc}$, which as shown in the broken line phasor of Fig. 5.15, lags $\mathbf{I}_a$ by 90 degrees. Thus the STATCOM has continued to operate as a capacitance.

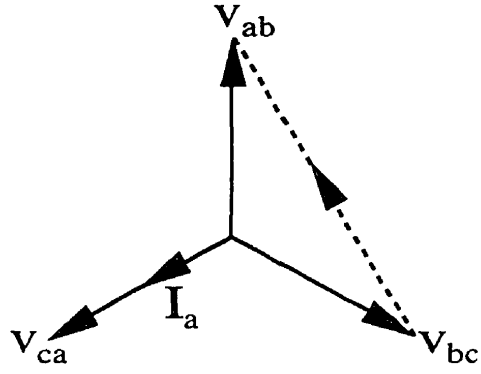


Fig. 5.15: Line-to-line voltage phasors of STATCOM with respect to $\mathbf{I}_a$.

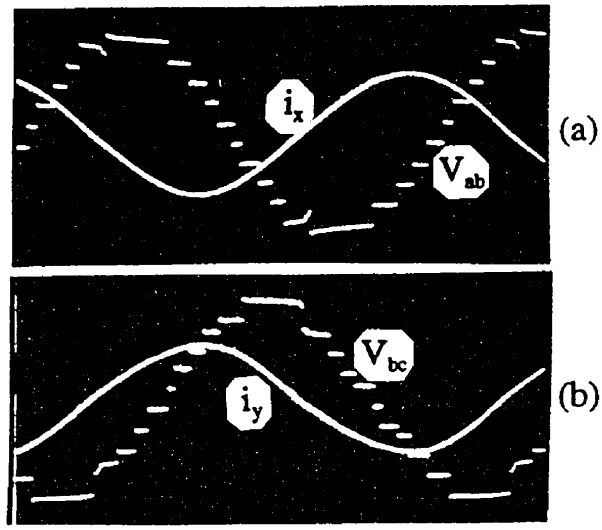


Fig. 5.16: Single-line Outage with neutral open. Transformer secondary voltages and currents. (a) $\mathbf{V}_{ab}$ and $\mathbf{I}_x$ (b) $\mathbf{V}_{bc}$ and $\mathbf{I}_y$

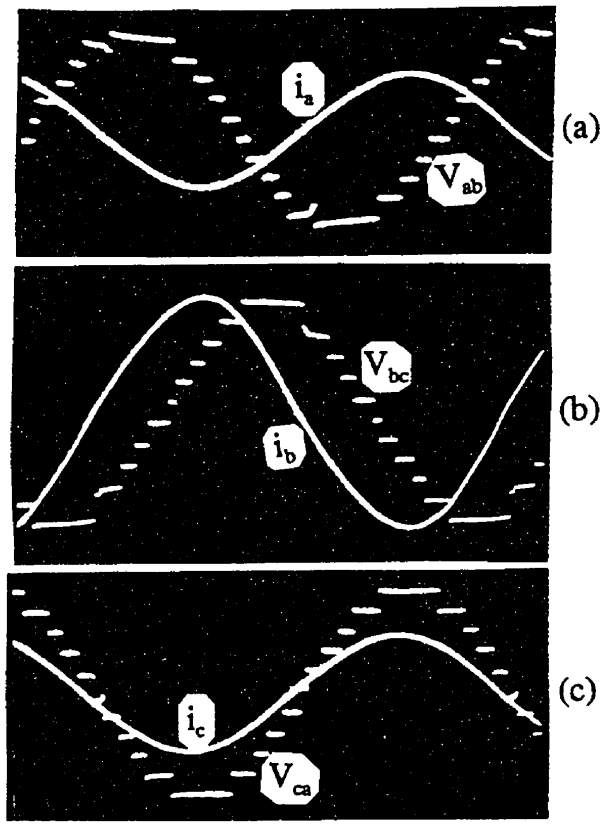


Fig. 5.17: Single-line Outage with neutral open. Converter-side-line voltages and currents. (a) $\mathbf{V}_{ab}$ and $\mathbf{I}_a$ (b) $\mathbf{V}_{bc}$ and $\mathbf{I}_b$ (c) $\mathbf{V}_{ca}$ and $\mathbf{I}_c$

5.6.4 DC Voltage Regulation Feedback

The STATCOM owes its robustness to the dc voltage regulation feedback loop, which advances or retards the phase angle of STATCOM voltages with respect to $\mathbf{V}_{ac}$ so as to invert or rectify sufficient real ac power to maintain the dc voltage at the regulated value while replacing ohmic losses. The delta connection of the transformer secondaries provides paths for the currents of the surviving lines to flow through the STATCOM which operates as single-phase or two-phase converters continue to charge the dc capacitors thus providing the "boost-strapped" power to maintain the dc link voltages and in return the ac voltages of the STATCOM. The equalization feedback plays its role so that the switches are equally stressed and the voltage waveforms are maintained.

5.7 Fail-safe Turn-off

The oscillogram of Fig. 5.18 shows the line currents when all the IGBTs in the 6-level converter are turned OFF simultaneously. There is no voltage spike because the secondary side currents continue to flow through the antiparallel diodes until they cross zero to reverse polarity. Fig. 5.18 shows the primary side currents which are the transformer magnetization currents after the turn-OFF. Turning-OFF is equivalent to inserting the large magnetization reactance of the transformers in series in the transmission line.

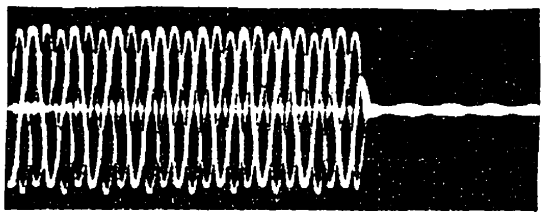


Fig. 5.18: Converter-side-line currents when the converter is turned off by disabling the switching signals.

5.8 Restoration of Series-STATCOM Operation

The oscillogram of Fig. 5.19 shows the line currents when the IGBTs in the 6-level converter are turned ON again after a turn-OFF of Fig. 5.18. It has been found that the lapse time for the successful restoration after a turn-OFF can be as long as 30 cycles. Failure to restore is related to the discharge of the dc link capacitor voltages by leaks and ohmic losses which are not replenished by "boot-strapping" operation of the dc voltage regulation loop.

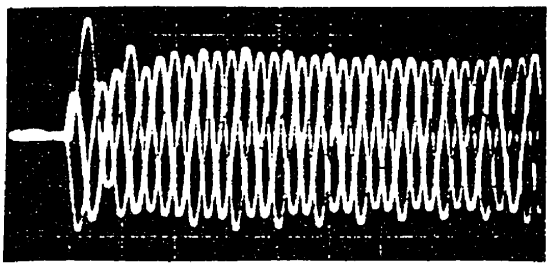


Fig. 5.19: Converter-side-line currents when the converter is restored into operation after been turned off.

5.9 Summary

The experimental research presented in this chapter has shown that multilevel STATCOM is feasible as a series STATCOM as it not only has the excellent feature for steady-state, normal operation but it has the robustness to cope with single-line and two-line outages. It has self-preservation features as fail-safe turn-OFF against faults and restoration. The chapter highlights the importance of the transformer delta-secondary connection.

In the next chapter, the method of eliminating the third harmonic on the dc capacitor voltages in multilevel converters will be presented.

CHAPTER VI

REDUCTION OF DC CAPACITOR SIZE BY USING 6-PHASE OR 12-PHASE AC

6.1 Introduction

In the previous chapter, the research has been oriented to the experimental evaluation of the multilevel STATCOM operating as a series-STATCOM. The success in the laboratory tests has increased the field of application from shunt-STATCOM to series-STATCOM. In this chapter, the objective is to address an inherent problem in the multilevel topology which, up to the present, has been glossed over.

The problem is presently hidden by using large size dc capacitors to make the inherent 3rd harmonic voltages in the dc link minuscule so as not affect the Total Harmonic Distortion Factors. Economically, it means that there is room to reduce cost by lowering the size of the capacitors provided the 3rd harmonic can be eliminated. In removing the 3rd harmonic, the peak dc link voltage of each level is brought closer to the average so that the voltage rating of the GTOs is employed more effectively. The 3rd harmonic also presents problems in designing the feedback loops for the dc voltage regulation and for the equalization of the dc capacitor voltages of the different levels of the converter. Presently, the choosing of the right proportional and integral gain constants in the negative feedback loops is a matter of trial and error.

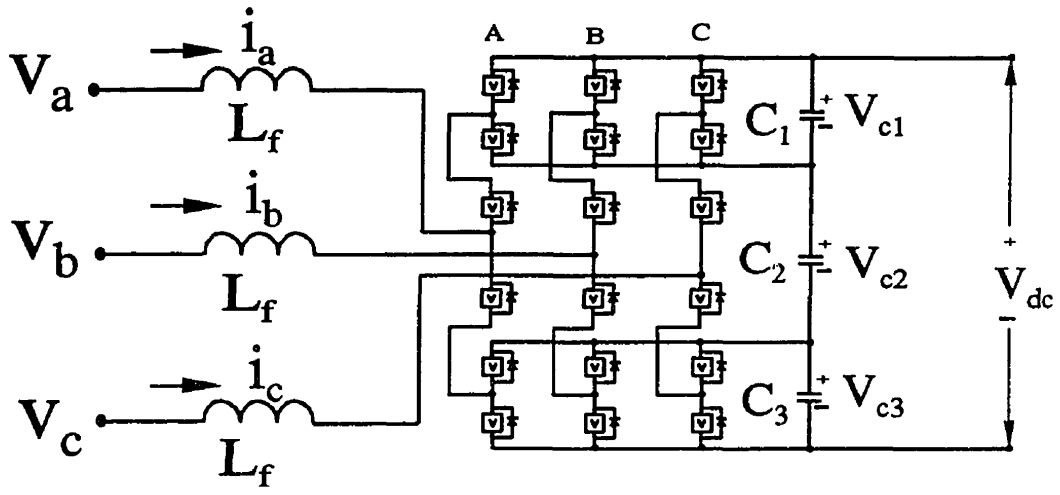


Fig. 6.1: Schematic of laboratory 4-level converter.

In this chapter, a method of eliminating the 3rd harmonic on the dc link capacitor voltages is presented. The method was verified experimentally using two laboratory 4-level converters operated as a 6-phase STATCOM. Fig. 1 shows the schematic of laboratory 4-level converter, used in the experimental tests. The simulation studies have been performed using diode-clamped 5-level converter shown in Fig. 6.2, which is the appropriate circuit for high voltage application as already explained in chapter V. The 6 phases are obtained from the standard 3-phase power supply by using two sets of 3-phase transformers, the polarities of the secondaries of the second set being reversed with respect to the first set. Thus when the phase angles of the first set are 0, -120 and -240 degrees, the angles of second set are: -180, -300, and -60 degrees. The angle between the phases is 60 degrees.

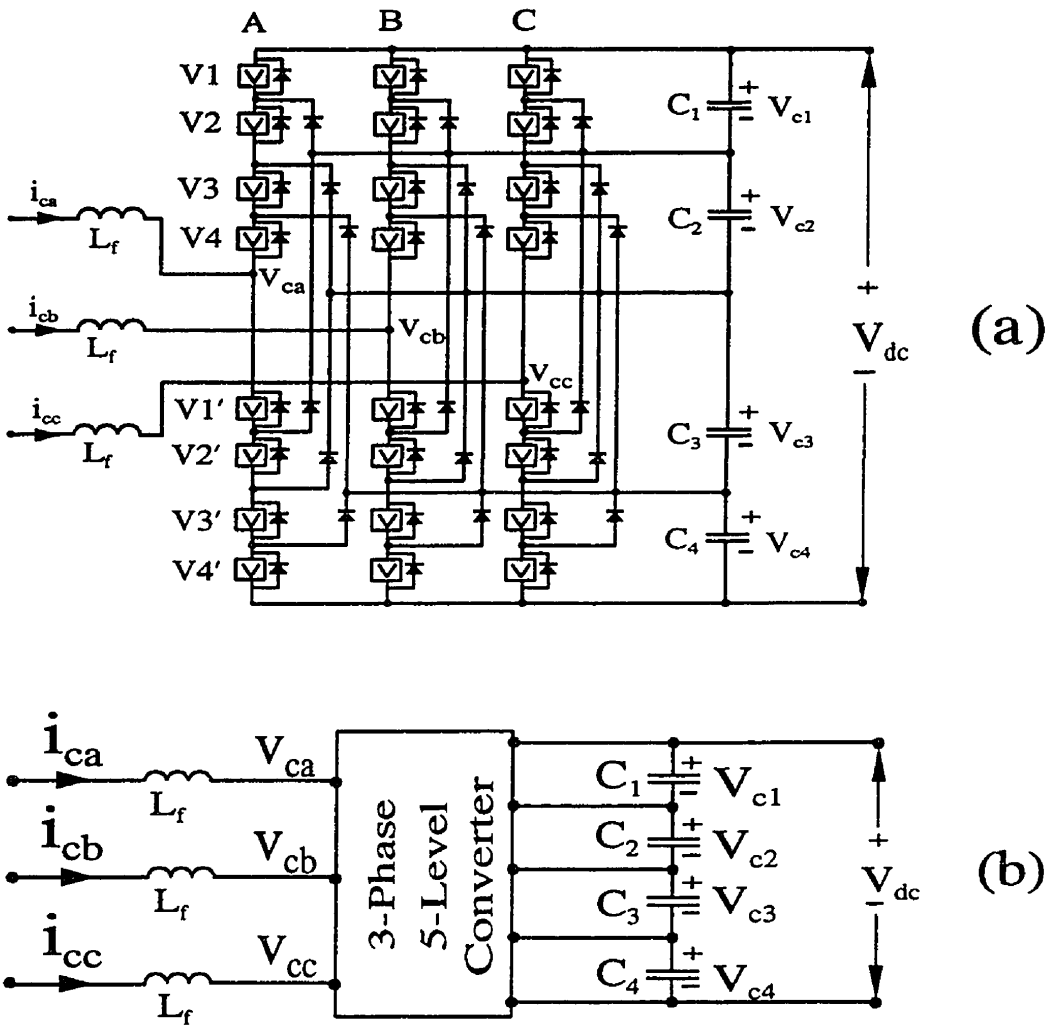


Fig. 6.2: Schematic of diode-clamped 5-level converter. (a) Schematic (b) Symbol.

Digital simulation also shows that the approach can be extended to eliminate the residual 6th harmonic when 4 multilevel converters are operated as a 12-phase STATCOM. The 12 phases are obtained by the wye/wye and delta/wye 3phase transformer arrangement to obtain the 30 degree shift between phases [32].

The inclusion of transformers needs some explanation as one advantage of the

multilevel STATCOM being vaunted is that it does not require transformers. Actually, this claim is made only for the 15 kV-size distribution shunt-STATCOMS. For the transmission line voltage ratings, step-up voltage transformers are inevitable. The requirement of 2 or 4 sets of three-phase transformers for the 6-phase or 12-phase systems respectively are justifiable for large MVA installations, because the cost of the transformers whether it is 1 set, rated at 1.0 pu MVA, or 2 sets, with each set rated at 0.5 pu MVA, or 4 sets, at 0.25 pu MVA, does not vary significantly. Thus, the savings in reducing the size of the dc capacitors are obtained with little cost.

6.2 Origins of Third Harmonics in dc Buses

In an ideal 2-level, bridge converter, the three ac terminals admit balanced 3-phase near sinusoidal currents into balanced 3-phase equivalent voltage sources so that the dc side outputs time invariant power. Why then, should one find in the multilevel converter such large 3^{rd} harmonic pulsating voltages in each of the multilevels? The answer lies in the fact that the solid-state switches of the upper half of Fig. 6.2(a) admit currents to the upper half of the capacitors only during the positive half of the ac cycle. Likewise the lower half of Fig. 6.2(a) is active only during the negative half of the ac cycle. This mode of operation means that the capacitor at any one level receives a rectified pulse current from one ac phase during one half cycle only. Fig. 6.3(a) illustrates the line current of the STATCOM and the conduction window, W, of one level of one phase. The current in Fig. 6.3(b) shows that under steady-state operation in the capacitive reactance condition, as much current is admitted into the dc link as is ejected in each cycle. The capacitor voltage, which is the time integral of the current of Fig. 6.3(b), is

displayed in Fig. 6.3 (c). The periodic voltage waveform of Fig. 6.3(c), v(t)=v(t-T), where T is the period, can be written in the Fourier Series as:

$$f(t) = Real\left\{\sum_{k=1}^{\infty} C_k exp[j2\pi k(t/T)]\right\} \tag{6.1}$$

where C_k is a complex Fourier coefficient and k being the Fourier harmonic number. The b- and c-phases produce identical waveforms except that they are delayed by T/3 and 2T/3 respectively. The total voltage is:

$$F_3[t] = f[t] + f\left[t-\frac{T}{3}\right] + f\left[t-\frac{2T}{3}\right] \tag{6.2}$$

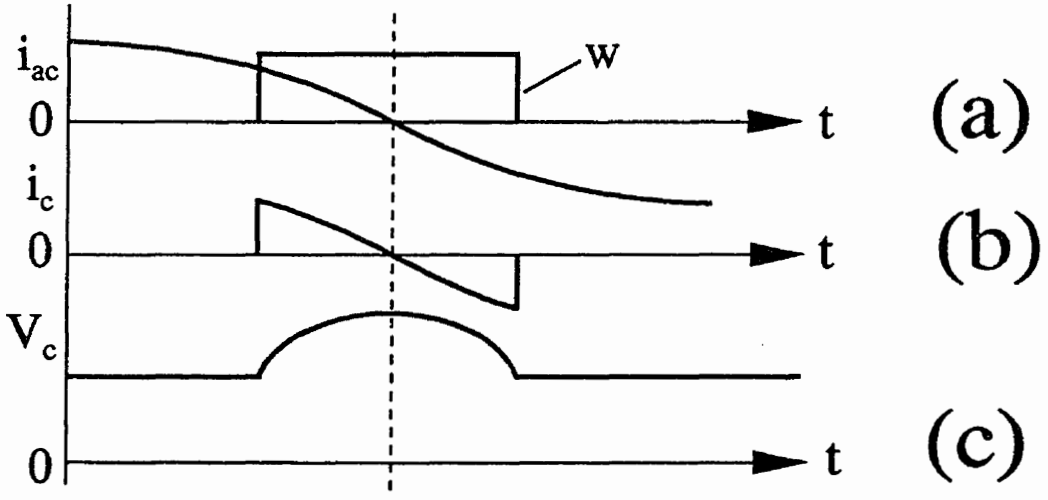


Fig. 6.3: Origin of third harmonic on the dc link when only one 3-phase STATCOM is used. (a) Line current and conduction window of one voltage level. (b) Dc Capacitor current due to one phase. (c) Dc capacitor voltage.

Writing $\theta=2\pi(t/T)$, $F_3(t)$ contains the summation

$$\exp[jk\theta] + \exp[jk(\theta-2\pi/3)] + \exp[jk(\theta-4\pi/3)] = 0 \tag{6.3a}$$

for $k \neq 3m$.

$$\exp[jk\theta] + \exp[jk(\theta-2\pi/3)] + \exp[jk(\theta-4\pi/3)] = 3\exp[jk\theta] \quad (6.3b)$$

for k = 3m.

Fig. 6.4(a) and (b) illustrate the summations of phasors of exp[jkθ], exp[jk(θ-2π/3)] and exp[jk(θ-4π/3)] of (6.3a) and (6.3b) respectively.

The Fourier Series of $F_3(t)$ is:

$$F_3(t) = Real\left\{\sum_{m=1}^{\infty} 3C_{3m}\exp[j2\pi(3m)t]\right\} \quad (6.4)$$

In general, one concludes that the dc capacitor voltage contains triplen harmonics, beginning with a large 3rd harmonic.

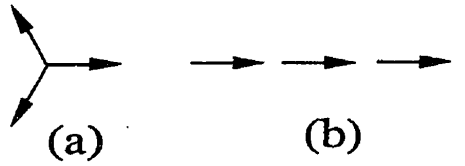


Fig. 6.4: Summation of exp[j2πk(t-nT/3)]. n = 1,2,3. (a) k ≠ 3m. (b) k = 3m. m = 1,2,...

6.3 Third Harmonics in Experimental Multilevel STATCOM

Fig. 6.5 is an oscillogram of the dc link capacitor voltage of one level of an experimental STATCOM, showing large 3rd and triplen harmonic ripples riding on the dc voltage. Fig. 6.6 displays the simulation results from a 3-phase, 5-level STATCOM, during a step change in the fundamental harmonic voltage magnitude control so that the STATCOM which has been delivering inductive VARs ends up delivering capacitive VARs. This change is apparent in the phase angle between the current with respect to the voltage in Fig. 6.6(a). Initially the current lags the voltage and then it changes over to become a leading angle. The 3rd harmonic is pronounced in the dc voltage in Fig. 6.6(b). The dc capacitors of [82] have been reduced in size so that the ripples are large and they affect the waveform of the ac output, V_{cal}, in Fig. 6.6(a).

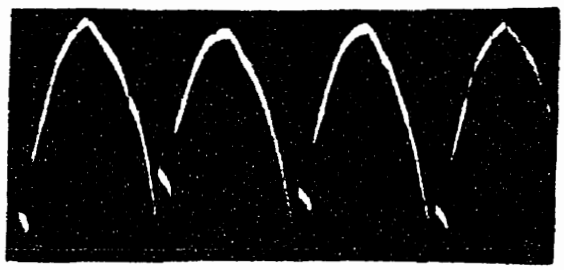


Fig. 6.5: Large 3rd harmonic on the dc link of one level when only one 3-phase STATCOM is used. Horizontal: 2ms/div. Vertical: 200mV/div.

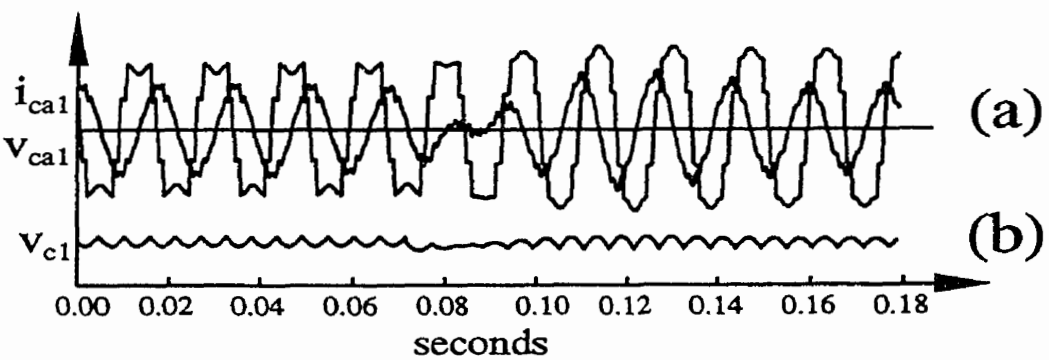


Fig. 6.6: Simulation results from a 3-phase 5-level STATCOM. (a) Ac voltage and current. (b) Dc voltage ripple across C_1.

Note that the 3rd and triplen harmonics in Fig. 6.6(b) have a waveform reversal in the transition from inductive to capacitive reactance operation. The changeover is apparent also in the ac voltage waveform of Fig. 6.6(a).

6.4 Elimination of Third Harmonics

From the trigonometric identities in (6.3), it follows that for a function periodic in T, g(t)=g(t-T),

$$G_6(t) = g[t]+g\left[t-\frac{T}{6}\right]+g\left[t-\frac{2T}{6}\right]+g\left[t-\frac{3T}{6}\right]+g\left[t-\frac{4T}{6}\right]+g\left[t-\frac{5T}{6}\right] \qquad (6.5)$$

contains harmonics which are integral multiples of 6 only, so that the 3rd harmonics are eliminated. The summation of the six exp[j2πk(t-nT/6)] (n = 1,2,..6), terms of the Fourier series yields the situation of Fig. 6.7(a) when k ≠ 6m which yields zero and of Fig. 6.7(b) when k = 6m which yields a sextet term. This principle can be applied to the STATCOM by using two identical multilevel converters which are both connected to the same dc buses as illustrated in Fig. 6.8. The ac power is derived from 2 identical sets of 3-phase transformers. The secondaries of the first set have 180° phase shift with respect to the second set.

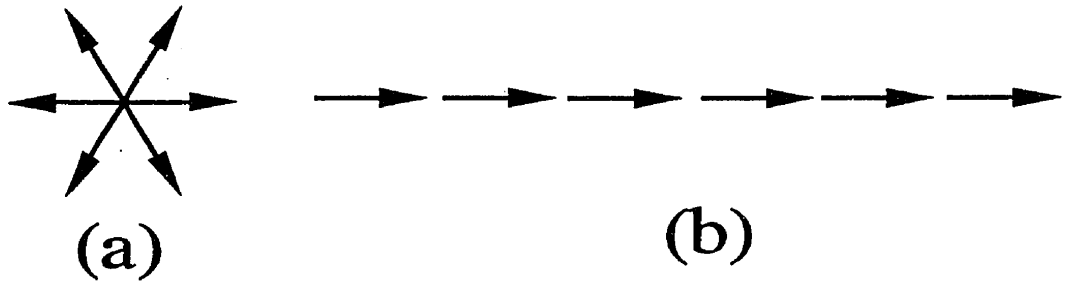


Fig. 6.7: Summation of exp[j2πk(t-nT/6)]. n = 1,2,..6. (a) k ≠ 6m. (b) k = 6m. m = 1,2,3,....

For the wye/wye connected six-phase arrangement shown in Fig. 6.8, one converter, the positive set identified by the subscript "1" receives 3-phase voltages at 0°, -120°, -240°. The second converter, the negative set identified by the subscript "2", receives 3-phase voltages at -60°, -180°, -300°. Note that the 60° phase shift of the fundamental frequency corresponds to 3 x 60° = 180° phase shift for the 3rd harmonic. Thus the 3rd harmonic pulses of the second converter will cancel those of the first converter in the dc links. This cancellation corresponds to the mathematical equation of (6.5) and the phasor diagram of Fig. 6.7(a)

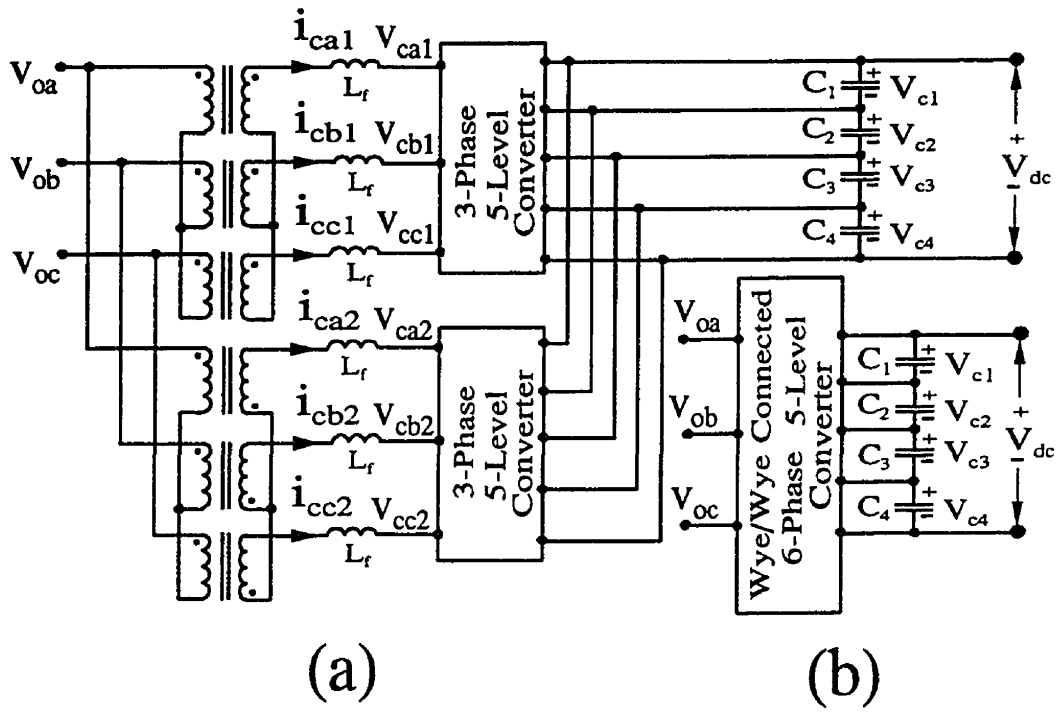


Fig. 6.8: Wye/Wye connected 6-phase 5-level converter. (a) Schematic. (b) Symbol.

6.5 Digital Simulation of 6-phase Multilevel STATCOM

The 6-phase, 5-level converters of Fig. 6.8 are designed to operate as a STATCOM using the controls which are shown in Fig. 6.9. The methods of control have already been described in [42,82,85] and only a brief summary is given here for completeness. The voltage magnitude control is through the "switching pattern" block which is a look-up table containing the switching angles of the fundamental frequency switching strategy which have been solved from a set of transcendental equations which specify the magnitude of the fundamental frequency voltage together with the elimination of low order harmonics. The voltage angles controlled through the "address register"

implement dc voltage regulation and equalization of the capacitor voltages.

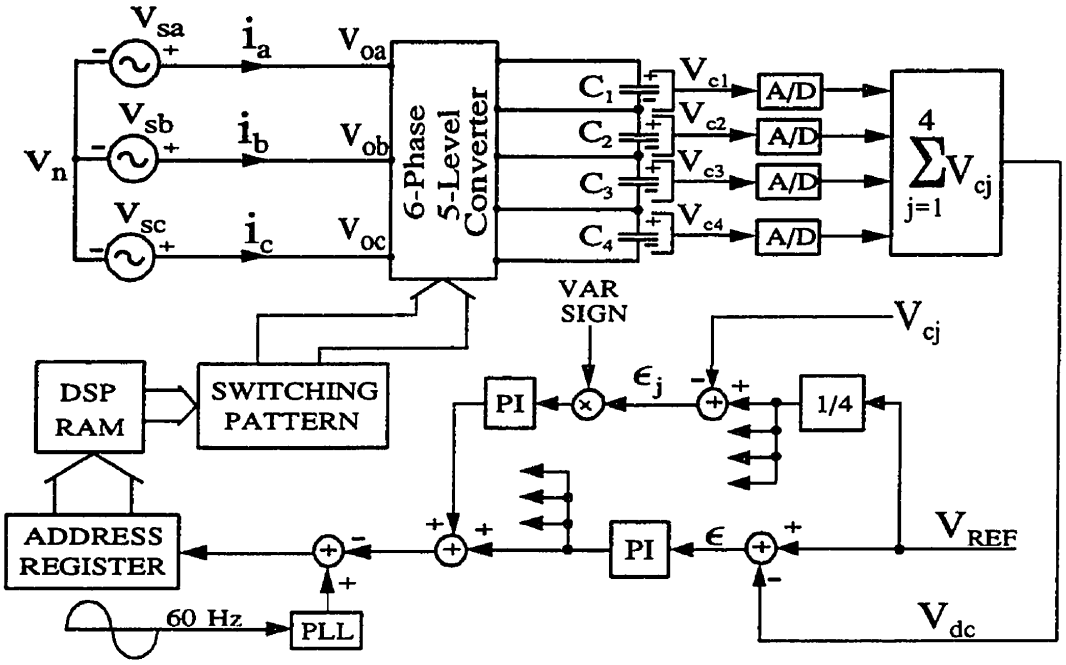


Fig. 6.9: 6-phase 5-level STATCOM.

Fig. 6.10 shows the digital simulation results of the 6-phase STATCOM under conditions which are identical to those in Fig. 6.6. Specifically, the same dc capacitor sizes are used. Fig. 6.10(a) and (b) show the voltages and currents of the positive and the negative converters respectively. Fig. 6.10(c) shows the dc link voltage of one level. Comparing Fig. 6.10(c) with Fig. 6.6(b), it is evident that the large 3rd harmonics are eliminated leaving residuals of the 6th harmonic. The 3rd harmonic distortions to the ac voltage outputs in Fig. 6.6(a) are not present in Fig. 6.10(a) and (b).

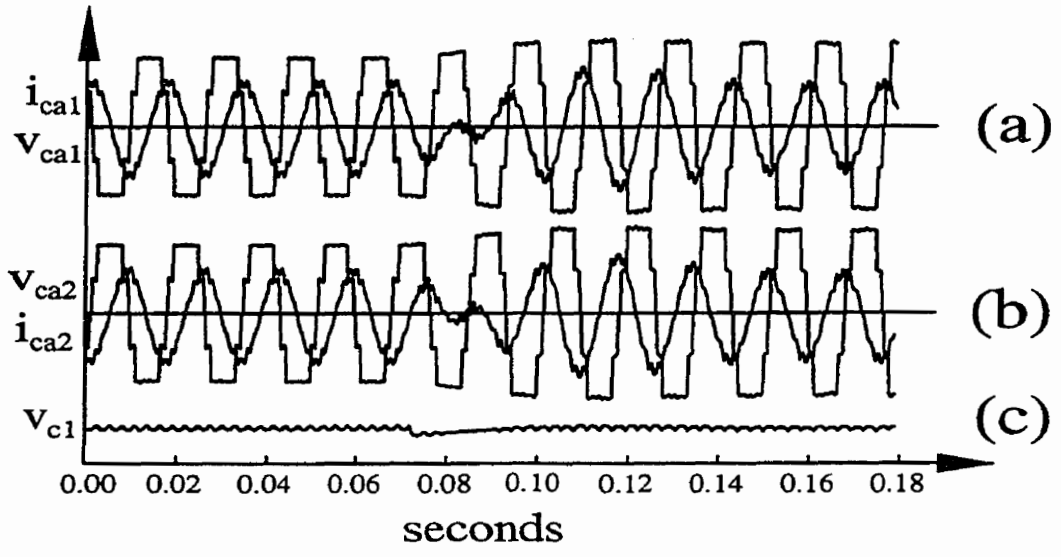


Fig. 6.10: Simulation results from a 6-phase 5-level STATCOM. (a) Ac voltage and current of the positive converter. (b) Ac voltage and current of the negative converter. (c) Dc voltage ripple across C_1.

6.6 Experimental Six-phase Multilevel STATCOM

From 6 modules of 3-phase IGBT bridges available in the laboratory, a 6-phase, 4-level STATCOM was realized. This consisted of 2 units of 3-phase, 4-level converters of Fig. 1, connected as shown in Fig. 6.8 and operated with controls similar to those shown in Fig. 6.9. The controls implemented dc bus voltage regulation and equalization of individual capacitor voltages. The 6-phases were obtained from 6 transformers arranged as shown in Fig. 6.8.

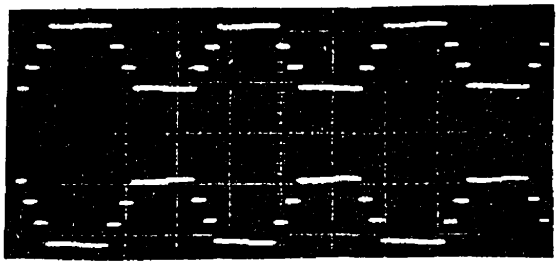


Fig. 6.11: Ac output waveforms of 4-level converters for 6-phase operation. (a) Positive converter. (b) Negative converter.

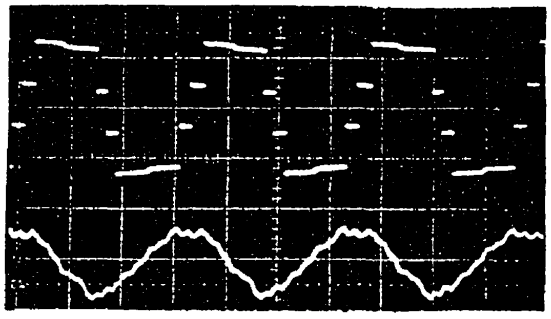


Fig. 6.12: Ac voltage and current waveforms of the 4-level converter at leading VAR operation. (a) Voltage. (b) Current.

The ac output voltages of the positive and negative converters are shown in Fig. 6.11. Fig. 6.12 displays the ac output voltage and current for one 4-level converter at leading VAR operation. Fig. 6.13 shows the total voltage and current on the transformer primary side. Fig. 6.14 and Fig. 6.15 show the residual 6^{th} harmonics for capacitive and inductive VAR operation as the 3^{rd} harmonic of Fig. 6.5 is eliminated. The same scale in the time axes is used in Fig. 6.5, Fig. 6.14 and Fig. 15.

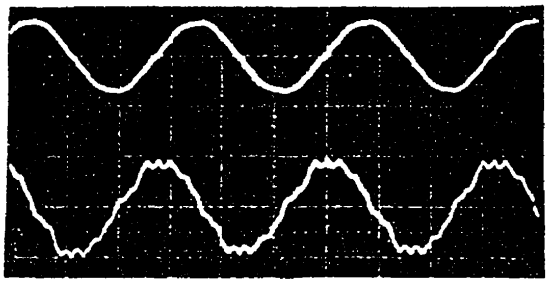


Fig. 6.13: Typical voltage and current waveforms of the 6-phase STATCOM measured on the power system side. (a) Voltage. (b) Current.



Fig. 6.14: Residual 6th harmonic on the dc link when 6-phase STATCOM is operated as capacitive reactance. Horizontal: 2ms/div. Vertical: 200mV/div.

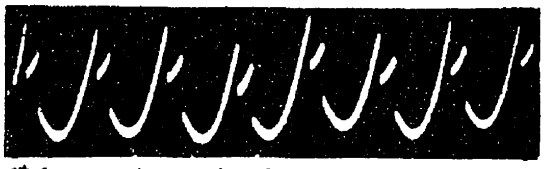


Fig. 6.15: Residual 6th harmonic on the dc link when 6-phase STATCOM is operated as inductive reactance. Horizontal: 2ms/div. Vertical: 200mV/div.

6.7 Twelve-phase Multilevel STATCOM

Continuing the method of harmonic elimination embodied in (6.2) and (6.5), the 6th harmonic can be cancelled by 12 identical voltages each time delayed by T/12, or phase shifted by 30 degrees. This practice has already been applied in DC Transmission Systems [32]. The 30 degree phase shift is obtained by the 2 sets of 3 phase transformers connected in the delta/wye arrangement shown in Fig. 6.16. The primary windings are connected in delta. Thus each primary winding has the line-to-line voltage applied across it. In comparison, the primaries of the transformers of Fig. 6.8 have the line-to-neutral

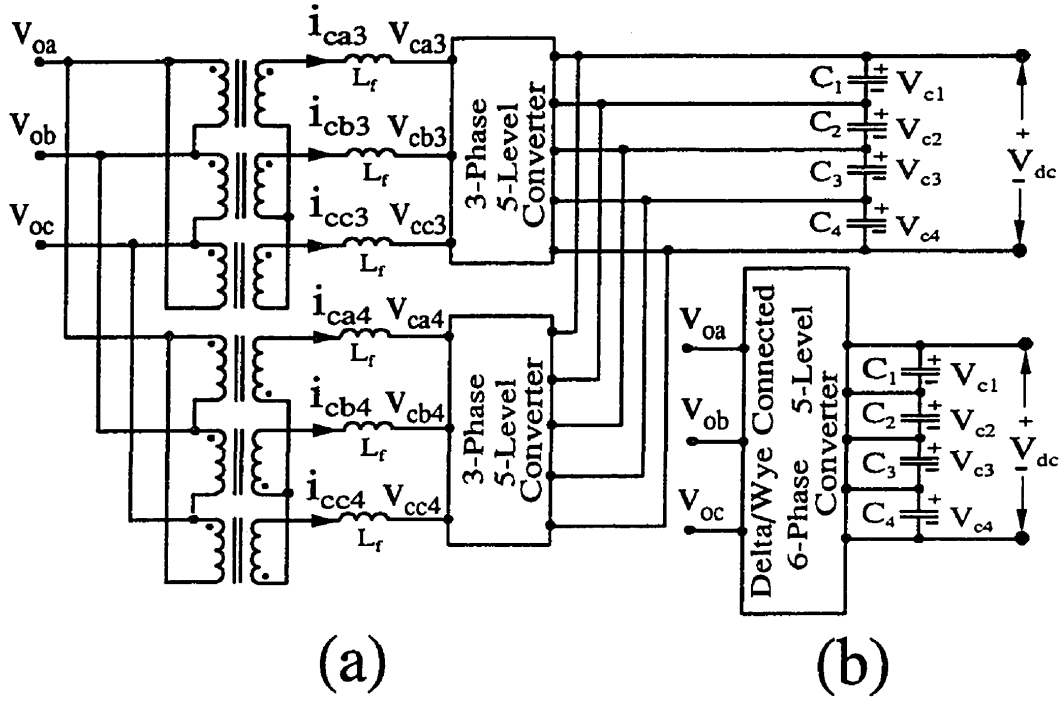


Fig. 6.16: Delta/Wye connected 6-phase 5-level converter. (a) Schematic (b) Symbol.

voltage across them. Fig. 6.17 shows the relation between the line-to-line voltages and line-to-neutral voltages. The line-to-line voltage $\tilde{V}_{ab}$, for example, is larger in magnitude by $\sqrt{3}$ and leads the line-to-neutral voltage $\tilde{V}_{an}$ by 30°. By increasing the primary turns of the transformers by $\sqrt{3}$ in Fig. 6.16, the secondary voltages have the same magnitudes as those in Fig. 6.8. A six-phase delta/wye system is formed in Fig. 6.16 by connecting the "undotted" terminals of the secondaries to form the "positive set" and the "dotted" terminals to form the "negative set" in the open wye configuration. The schematic for the wye/wye 6-phase is the same as illustrated in Fig. 6.8. Fig. 6.18(a) shows the voltage phasors of the 6-phase delta/wye system of Fig. 6.16.

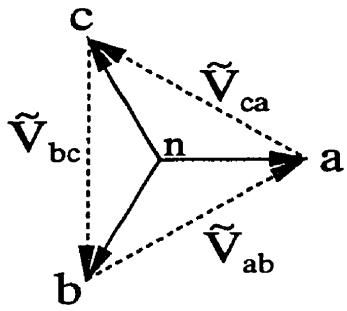


Fig. 6.17: Relationship between line-to-neutral and line-to-line voltage.

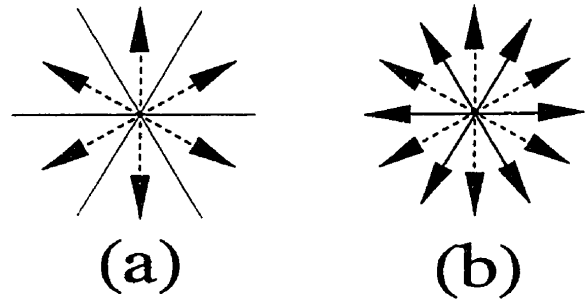


Fig. 6.18: Voltage phasors. (a) 6-phase delta/wye system. (b) 12-phase system.

The 12-phase system is formed from connecting the wye/wye system of Fig. 6.8 in parallel with the delta/wye system of Fig. 6.16 in the manner shown in Fig. 6.19. Fig. 6.18(b) shows the 6 voltage phasors (broken lines) of the delta/wye set bisecting the 6 voltage phasors (solid lines) of the wye/wye set. Altogether the system requires 4 multilevel converters each having its set of 3-phase transformers so that there are altogether 12 balanced phases.

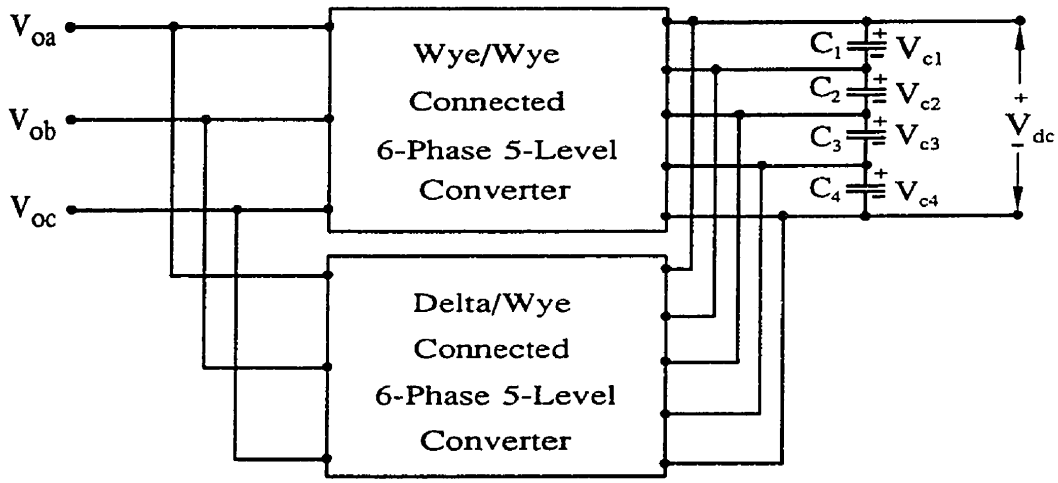


Fig. 6.19: 12-phase 5-level converter.

6.8 Digital Simulation of Twelve-phase Multilevel STATCOM

Fig. 6.20 shows the digital simulation results of the 12-phase multilevel STATCOM. The dc link capacitor voltage in Fig. 6.20(e) shows that the 6^{th} harmonics in Fig. 6.10 are eliminated, leaving residual 12^{th} harmonics. Fig. 6.6, Fig. 6.10 and fig. 6.20 are simulations of the same reactive power reversal.

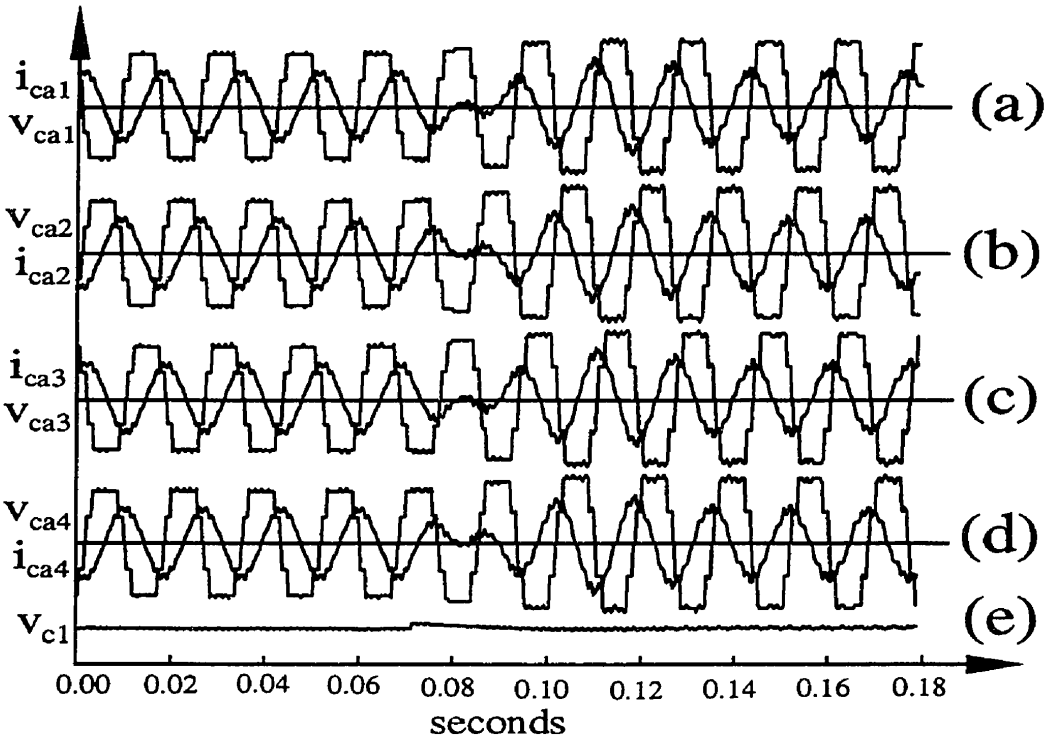


Fig. 6.20: Simulation results from a 12-phase 5-level STATCOM. (a) Voltage and current, wye/wye positive converter. (b) Voltage and current, wye/wye negative converter. (c) Voltage and current, delta/wye positive converter. (d) Voltage and current, delta/wye negative converter. (e) Dc voltage ripple across C_1.

6.9 Discussions

By comparing the capacitor voltage waveform, V_{c1} in Fig. 6.6, Fig. 6.10 and Fig. 6.20, one sees the improvement as the third and the sixth harmonics are eliminated.

The judgment of utility users and manufacturers will have to be sought in determining if the sixth harmonic can be tolerated. The 12-phase system is at hand in reserve to reach a higher level of perfection.

Using the waveforms of the 6-phase system of Fig. 6.10 as the basis for comparison, digital simulation shows that in order to reach the same quality using the 3-phase system of Fig. 6.2 alone, the dc capacitor sizes have to be increased by a factor of 4. Thus the saving in capacitors is not insignificant. However, this must be balanced against the transformer cost and the increased circuit complexity.

For high MVA applications, multiple modules of multilevel converters and multiple transformer sets are not added costs. When the current ratings require GTOs to be paralleled, this can be done either as devices in parallel or as modules in parallel. Likewise, transformer cost is based on MVA rating. Thus the transformer cost does not change significantly as to whether a 3-phase, 6-phase or 12-phase system is considered when their total MVA is not changed.

6.10 Summary

In this chapter, it has been revealed that the 6-phase and the 12-phase multilevel STATCOM eliminate the third and the sixth harmonics thereby enabling the dc capacitor sizes to be reduced, while meeting THD standards. In addition, the voltage peaks at each level of the dc link is lowered so that they approach the average dc voltage. Consequently, the voltage rating of the GTOs can be more gainfully employed to produce a higher ac voltage. Thus there is a cost advantage.

CHAPTER VII

CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK

7.1 Summary

The goal of the research of the thesis is to develop the methodologies necessary for the integration of the solid-state switches (the highest power solid-state switch, the GTO, is presently rated at 6kV, 6kA) so that the FACTS controllers have the voltage withstand (in the order of 500kV) and the current carrying capacity (ratings at hundreds of MVA). The FACTS controllers are based on converter modules or multilevel modules as the building blocks from which the series-STATCOMs, the shunt-STATCOMs and the Unified Power Flow Controllers (UPFC) can be realized. The FACTS controllers function as modulators of real and reactive power to increase the transmission capacity of the electric power utilities without the necessity to build new transmission lines.

The underlying threads which weave the chapters together consist of the several promising technologies and methodologies, which have to be mastered, in order to synthesize the FACTS controllers. The technologies and methodologies have been taken from many sources. They fall under the following headings:

(1) Converter Topologies

The converter topologies are limited to the two most promising:

(a) 2-level, voltage-source converter-Chapter II and III.

(b) diode-clamped, multi-level converter-Chapter IV, V and VI.

(2) Switching Strategies

Two control strategies have been the mainstay of the research. They are:

(a) the Phase-Shifted Triangle Carrier Technique of the Sinusoidal Pulse Width Modulation Strategy-Chapter II, III, and IV.

(b) the Fundamental Frequency Method-Chapter V and VI.

(3) Integration Technology

The converter modules are all connected in parallel at their **dc links**. The three general methods of integrating the multi-modules at their **ac terminals** are:

(a) parallel connection-Chapter II, IV.

(b) series connection-Chapter II, III.

(c) parallel connection of series-connected modules-Chapter II.

(4) Transformer Technology

Transformers give the galvanic isolation necessary for the series connection of modules. By wye-wye and wye-delta transformer arrangements, 6-phase and 12-phase ac systems can be produced from the standard 3-phase ac power supply. In the thesis, the transformers have been used for:

(a) galvanic isolation-Chapter II, V and VI.

(b) production of 6-phase and 12-phase ac systems-Chapter VI.

(5) Digital Methodology

The digital (DSP) control of the array of modules requires an interface, which in the perfected form takes the name "7-Timer Method". The 7-Timer Method, which has been described in Chapter III, has made it possible to obtain the experimental results in Chapters II and III.

Part 1, consisting of chapters II and III, and **Part 2**, consisting of chapters IV, V

and VI, are devoted to the two converter-topologies covered by the thesis. As the 2-level, voltage-source converter topology of Part 1 is a relatively, mature technology, what remains to be done consist of giving experimental proof to previous publications of digital simulation results [35,36]. The more recent, diode-clamped, multilevel converter topology of Part 2 requires extensive research before it can be commercially marketable.

The conclusions of the thesis have been verified by digital simulations in the first instance. More solid verifications come from experimental tests in laboratory models. A good portion of the research effort has been devoted to the planning, designing, and building of 6 modules of 3-phase, 5kVA-size, IGBT, voltage-source converters, which now form a major part of the Multi-Converter Test Facility in the Power Electronic Laboratory. The Appendixes contain descriptions of the Test Facility. The design and the building of the data-acquisition system and the real-time multi-DSP controller platform have been the work of Dr. Zbiegnew Wolanski, who is the co-author of the many publications. As the first user, the candidate has to trouble-shoot, debug and commission the Multi-Converter Test Facility.

7.2 Conclusions

PART 1 2-LEVEL CONVERTER TOPOLOGY

Chapter II is concerned with using multi-modules of 2-level converters to realize the MVA FACTS controllers. The method of control is by the phase-shifted triangle carrier technique of the Sinusoidal Pulse Width Modulation (SPWM) strategy, which has the advantage that the effective carrier frequency is increased by a multiple of N, the number of converter modules forming the array. It has the important implication that slow

power switches (GTOs) can benefit from the advantages of the SPWM strategy, because the low switching rates can be compensated by using large numbers of modules. Unfortunately, for the very low rate of 3 pulses per modulating cycle suitable for the GTOs, the output ac voltages from the modules are not equal so that they cannot be connected directly in parallel without serious current unbalance. The main research effort is devoted to finding ways of equalizing the converter currents.

Three important conclusions are reached from both digital simulations and laboratory experiments.

- It is possible to form groups of 4 GTO-converters in series which can be connected in parallel at their ac terminals without current unbalance.
- For IGBT-converters, which can switch at 12 pulses per modulating cycle or higher, the modules can be connected directly in parallel.
- Series connections of converter modules require magnetic transformers for galvanic isolation. Series cancellation of harmonic noise voltages is preferred to parallel cancellations of harmonic noise currents, as the inductive filter does not have to be large.

The conclusions are significant as they say that the SPWM-FACTS controllers are realizable by high power solid-state switches ranging from the slow GTOs to the fast IGBTs.

Although the transformer adds to cost, its cost must be balanced against that of the inductive filter, which is custom-designed and tends to be expensive as it has no other market demand. If an off-the-shelf, mass-market transformer can be found which fits the

design constraints, cancellation as harmonic voltages may be cheaper than direct parallel connection, requiring inductive filters.

Chapter III brings digital technology to the control of the array of multi-modules. The Sinusoidal Pulse Width Modulation (SPWM) strategy has been conceived for analog circuits. The application of phase-shifted triangle carrier technique has introduced a further complication of using low triangle carrier frequency (so as to be compatible with slow switches such as the GTOs) while encoding information at a faster sampling rate (to increase bandwidth). A solution has been found under the name, the "7-Timer Method", which uses the "crossed diagonals cells" (formed from the grid of the triangle carriers) to translate the "natural sampling" in the SPWM strategy to "regular sampling" of digital technology. The "7-Timer Method" has been implemented using a Texas Instruments TMS320C40 DSP in conjunction with a FPGA device. All the experimental results in Chapter II have been obtained using the "7-Timer Method" to control the converter modules. Thus, the following conclusion can be made, with confidence:

- The "7-Timer Method" enables the FACTS controllers to be controlled digitally.

This is an important capability because many modern control and active filtering methods involve computational algorithms. The array of 2-level converter modules responds under the control of the "7-Timer Method" as 3 high power linear amplifiers, with a high constant gain, without phase-shift.

PART 2 DIODE-CLAMPED MULTILEVEL TOPOLOGY

Chapter IV: This thesis has regarded the diode-clamped, multilevel converter as having important potential for applications in STATCOMs, using the slow GTOs as switches. Presently, the successful and favored control strategy is the "Fundamental Frequency Method". A nagging question is why the SPWM strategy, used so successfully in the 2-Level Converters, such as in Chapter II, is not used in the diode-clamped, multi-level converter. As the diode-clamped, multi-level converter is a recent topology, some time is taken to answer the question as part of fundamental research. The conclusion is that:

- In applying the SPWM strategy, the frequency of the triangle carriers needs to be very much higher in the multi-level converter than in the 2-level converter.

To overcome this impasse, multi-modules of diode-clamped, multi-level converters have been explored. From the results of simulation studies using 8 modules of 5-level converter, the following conclusions are made:

- The SPWM strategy can be implemented using one triangle carrier per modulation cycle, when multi-modules of the diode-clamped, multi-level converters operate under the phase-shifted triangle carrier technique. The voltage THD is low and the input/output linearity is good.
- The switching loss is the lowest at one pulse per modulating cycle. The SPWM strategy enables the array to function as 3 high power high gain linear amplifiers.

Chapter V: This chapter considers the application the diode-clamped, multi-level converter as a series-STATCOM to compensate the large inductive reactance in the radial

transmission-line joining the sending-end bus to the receiving-end bus. It should be mentioned that there has already been several studies on the shunt-STATCOM [40,54,44,55,63,82,85], where the vaunted advantage is that in distribution voltage levels in the region of 15kV, there is no longer the need of the transformer stage because the voltage level can be reached by 5 to 7 levels of GTOs.

In the series-STATCOM, magnetic transformers are needed for the galvanic isolation to insert the compensating voltages in series with the transmission lines. Although transformer technology is well established, nevertheless experimental spot-checks are necessary to verify that there is no unexpected difficulty associated with transformer connections.

Another reason for the spot-checks follows from the topological difference in the 3-phase network assumed in the simulation and laboratory tests on the shunt-STATCOM. Because the researchers of the shunt-STATCOM [44] come from a background of power electronic drives, the wye connection has been assumed in their studies as a matter of course. In the series-STATCOM application, however, the converter has to be connected to transformer secondaries connected in delta. This configuration is required to allow the zero-sequence of the transmission lines (during faults) to find a path as the circulating currents through the delta connected secondaries.

The laboratory facilities for carrying out the spot-checks are conveniently suitable for finding out as to how well the series-STATCOM withstand unbalanced conditions. For this reason, an experimental program was carried out to understand how the series-STATCOM survives loss of line(s). From the experimental test results, the following conclusions are made:

- The filtering effects of the large series line inductance enables the series-STATCOM to have better current waveforms than the shunt-STATCOMs.
- The delta connection of the transformer windings on the converter side, provides a path for the zero sequence currents during transmission line faults.
- The same delta connection enables the STATCOM to continue compensating in the remaining intact line(s), in the event of a loss of a single line or loss of double lines. In the duration of the fault(s), the dc voltage regulation feedback and the equalization feedback continue to function through the intact line(s).

Chapter VI: returns from research in application as a STATCOM in Chapter V to research in improving the performance of the diode-clamped, multilevel converter by strengthening the design. The diode-clamped, multi-level converter has an inherent 3^{rd} harmonic voltage component on the dc link side in each of the multi-levels. The effects of the 3^{rd} harmonic are presently minimized by connecting large dc capacitors.

The 3^{rd} harmonic elimination is achieved by summing the dc outputs of two modules which are phase shifted by 60 degrees. This leaves the 6^{th} harmonic, which again can be eliminated by adding paired outputs which are shifted by 30 degrees. The 60 or 30 degree phase-shifts are obtained from wye-wye and wye-delta connections of 3-phase transformers to form a 6-phase or 12-phase system. This research yields the following conclusions:

- Two modules of multi-level converters, supplied by a balanced 6-phase ac system, eliminate the 3^{rd}-harmonic component, leaving the 6^{th}-harmonic, at the dc link voltages.

- Four modules of multilevel converters, supplied from a balanced 12-phase ac system, eliminate both the 3rd and 6th-harmonics, leaving behind the 12th-harmonic, in the dc link voltages.

The successive eliminations of the 3rd and then the 6th harmonics allow the dc capacitor sizes to be reduced. Furthermore, the average dc voltage as a percentage of the maximum voltage in the dc link capacitor increases so that the insulation is used more effectively. This gain has to be balanced against the complexity of the 6-phase or 12-phase ac systems. As the cost of the transformers is tied to the MVA ratings and not to the count of the transformer units (which increase from 3 to 6 and then 12), there is a nett gain as the cost of the capacitors is effectively reduced.

7.3 Suggestions for Future Work

Opportunities of future work consist of consolidating the advances made in the chapters of the thesis:

Chapter II-The qualitative study can be followed by the development of analytical formulations, for designers to use in quantitative evaluations and optimization studies.

Chapter III-The sample-and-hold signal processing of the 7-Timer Method can be improved by approximating the modulating signal by a straight line joining the samples at t_{k-1} and t_k. The times t_{on} and t_{off} can be computed from triangulation. This new method will lead to better accuracy.

Chapter IV-The phase-shifted triangle carrier technique of the SPWM strategy, applied to multiple modules of multi-level converter at the rate of only one triangle carrier per modulation period, does not have a theoretical foundation. The excellent simulation

results suggest that there is an analytical basis in the harmonic cancellations.

- Further research is required to find ways to equalize the currents in the different modules.

Chapter V and VI - Incorporation of the 6-phase and 12-phase ac systems to the design of the series-STATCOM and the shunt-STATCOM.

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Appendices

APPENDIX A

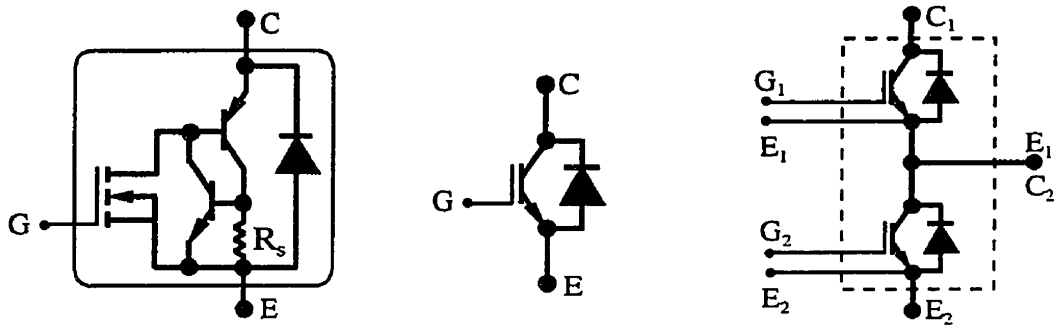
MODULAR CONSTRUCTION OF POWER CIRCUIT

A.1 Introduction

The power circuit of the experimental facility consists of six modules of 3-phase IGBT Converters. The modules have been constructed for easy inter-changeability and configuration of different power circuit topologies. Each 3-phase bridge has been made using 3 IGBT half-bridge power modules. The modular construction made possible to conceive multiconverter system, 6-level converter and two sets of 4-level converters which were used for 6-phase experimental tests.

A.2 Half-Bridge IGBT Power Module

The half-bridge IGBT power module is the building block of the power circuit in the experimental facility. The half-bridge power module is composed of 2 IGBT with internal antiparallel diodes. Each IGBT is rated 600V maximum Collector-Emmiter voltage and 50A collector current. The part number of the half-bridge power module is CM50DY-12H from POWEREX company. Fig. A.1 shows the outline of the power module. More details can be found in the data sheets [66,86].

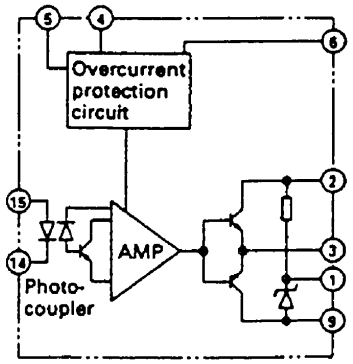


Equivalent circuit Symbol Half-Bridge module

Fig. A.1: Insulated Gate Bipolar Transistor (IGBT), Part. No. CM50DY-12H.

A.3 Gate Drivers for the IGBT Switches

Commercially available IGBT gate drivers have been used. The part No. of the gate drivers is EXB841, 15 pin sip package, hybrid integrated circuit from FUJI company. The gate driver is capable of delivering a peak current of 4A. The gate drive capacity is adequate for up to 600V, 300A IGBT device. It consists of galvanic isolation of 2500V provided by opto-isolator. It has built in overcurrent protection circuit which is an important feature for short circuit protection of the IGBT. The overcurrent signal is available for use in the controls through galvanic isolation. It has internal circuit to split the supply voltage of 20V into +15V for switching ON state and -5V for switching OFF state. Fig. A.2 shows the functional block diagram and pin out description. More details are available in the data sheets [66,87].



Pin number	Description
①	Connected to smoothing capacitor for reverse bias power supply
②	Power supply (+20 V)
③	Drive output
④	For connecting an external capacitor to protect against malfunction of the overcurrent protection circuit. (The capacitor is not needed in most cases.)
⑤	Overcurrent detection output
⑥	Collector voltage monitoring
⑦ ⑧	Not connected
⑨	Power supply (0 V)
⑩ ⑪	Not connected
⑭	Drive signal input (–)
⑮	Drive signal input (+)

Fig. A.2: Functional Block Diagram of EXB841 IGBT Gate Driver from FUJI.

A.4 Isolated Power Supplies for the Gate Drivers

Since the experimental facility has been designed for multipurpose use, it was necessary to have each of the IGBT gate drivers powered from isolated power supplies. Due to low gate drive power requirement of the IGBTs, it was possible to use compact power supplies, with 2W output power, which are commercially available. The part number of the power supplies is PWR316 high frequency DC/DC converter type from Power Convertibles company. Each power supply module has 2 outputs which are isolated from each other and from the input at 3000V. Therefore, each of the power supply module was used to power 2 gate drivers for the half-bridge power module. As a result, 3 power supply modules were used to supply 6 gate drivers of the 3-phase bridge. The

input voltage to the power supply modules was obtained from the mains through a small transformer, rectifier and variable output voltage regulator. Using LM317, the input voltage to the power supply modules was tuned such that their output were at 20V which is the requirement of the FUJI gate drivers. Fig. A.3 shows the outline the PWR316 power supply modules from Power Convertibles company. More details can be found the data sheets [66,88].

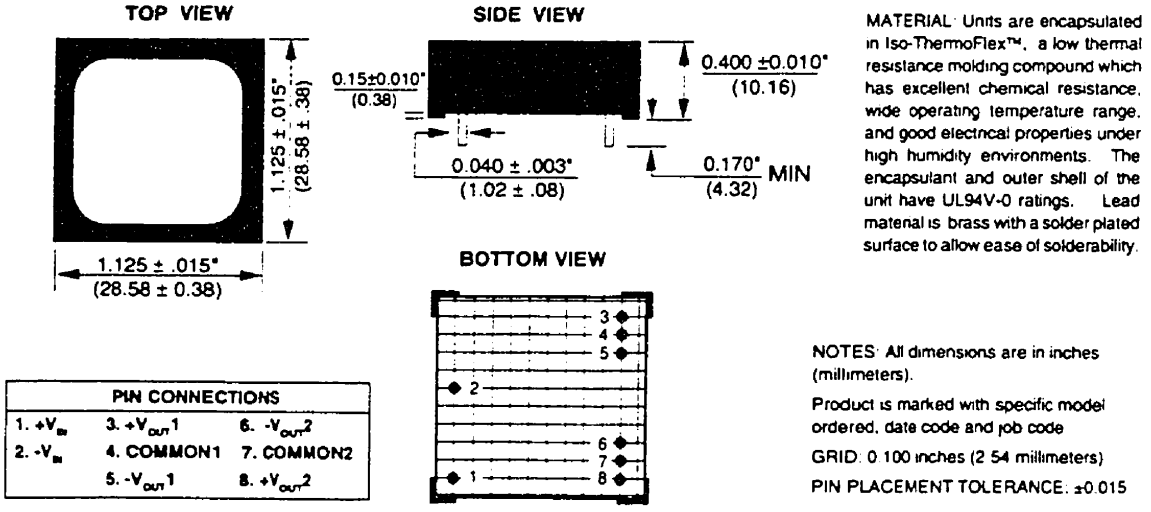


Fig. A.3: Outline of PWR316 Power Supply Modules from Power Convertibles.

A.5 Interlock circuit

Interlock circuit is provided so that two power switches, in voltage source type of converters, in a single leg can not be in "ON" state simultaneously. This is done to avoid shoot through across the DC capacitor. In order to reduce the number of control signals from the digital controller, the interlock and splitting of the three phase signal have been implemented on the gate drive board. The Programmable Logic Device (PLD) has been programmed to receive four control signals from the digital controller, three signals are

for the 3-phases and the fourth signal is for enabling the switching signals to the gate drivers. The enable signal is common for all modules of the 3-phase converters. Table A.1 displays the ORCAD source program for the PLD. Fig. 4 shows the schematic of the Gate Driver Board (GDB) for one module of 3-phase converter. The GDB has been implemented on the Printed Circuit Board (PCB) which is shown in Fig. 5.

Table A.1: List of PLD program for 3-to-6 signal splitting and interlock.

```
*******************************************************************************
* Name: PWM1.PLD                                                              *
* Function: 3-to-6 signal splitting and interlock for 3-phase voltage source converter  *
*******************************************************************************
GAL16V8A     in: ( A, B, C),
             io: Q[0..5],
             clock:clk
             Title:"firing circuit"
             Q0 = clk // (A & Q1')
             Q1 = clk // (A' & Q0')
             Q2 = clk // (B & Q3')
             Q3 = clk // (B' & Q2')
             Q4 = clk // (C & Q5')
             Q5 = clk // (C' & Q4')
vectors:
 {Display ( clk, A, B, C, Q[0..5] )c
 test A = 1(1,0); B = 2 (1,0); C = 4(1,0); clk = 5(0,1)
 End}
```

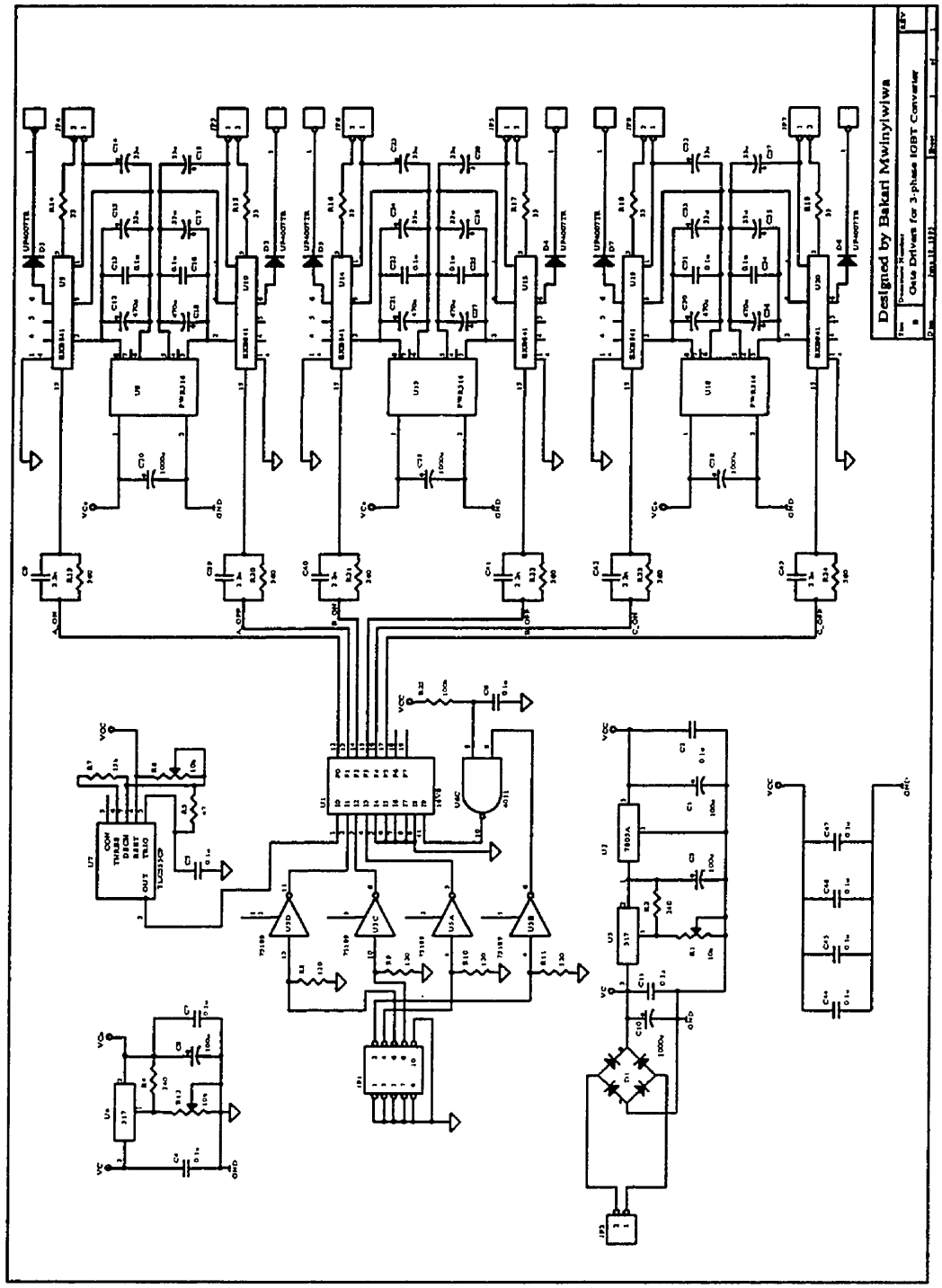


Fig. A.4: Schematic of the Gate Drive Board for 1 module of 3-phase converter.

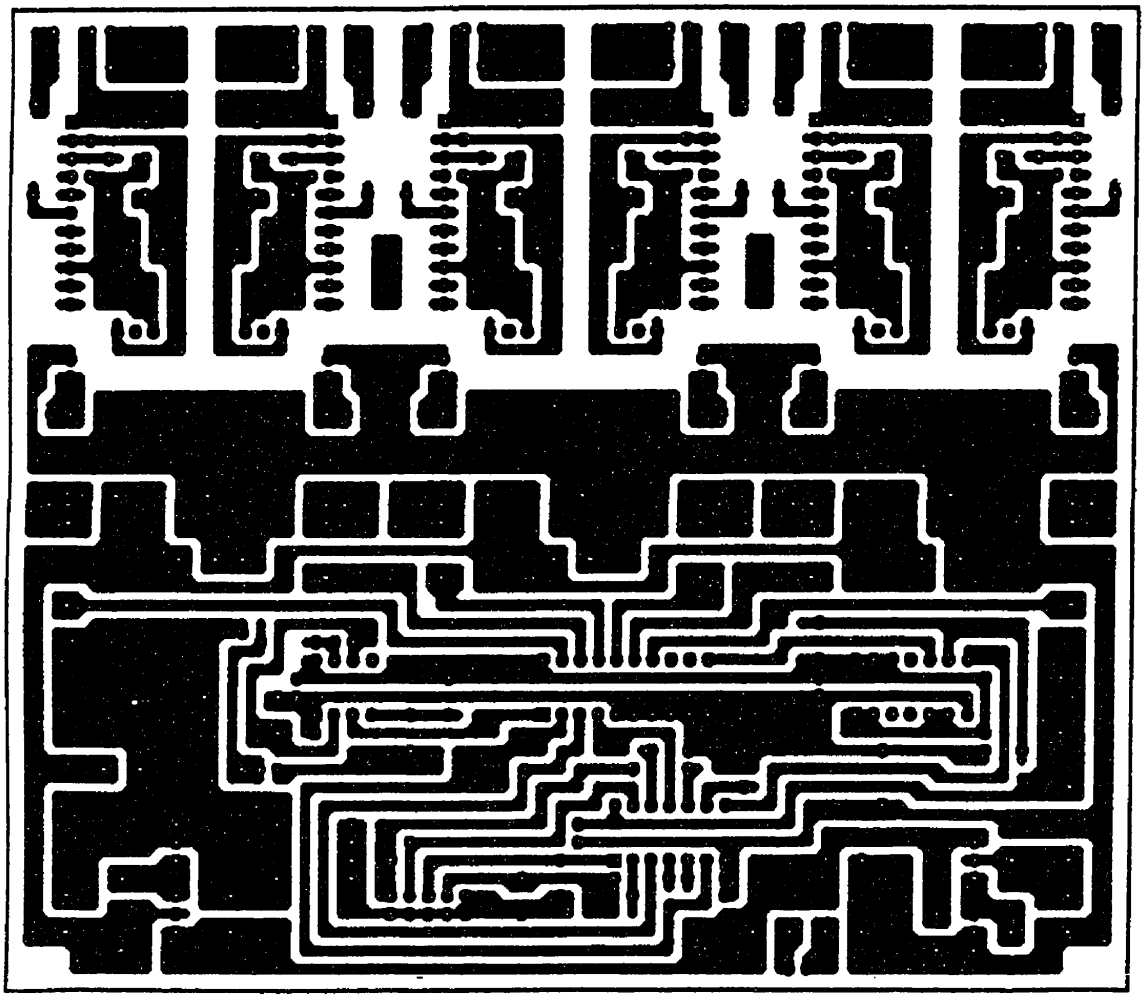


Fig. A.5: Gate Drive Board PCB for 1 module of 3-phase converter.

A.6 Physical Layout of one Module of 3-phase Converter

Each module of 3-phase converter has been mounted on an aluminium perforated sheet. The single module assembly consist of:

(1) Three half-bridges of IGBT power modules mounted on the heat sink.

(2) Gate drive PCB board.

(3) Rectifier transformer for power supply of the gate drive circuitry.

(4) Two DC capacitors for DC link.

(5) Data acquisition boards' (A/D boards) holder which can accommodate up to 5 PCBs.

(6) Shunt Resistor holders which can accommodate up to 5 resistors for current measurement.

(7) Two terminal blocks, one in front and one at the rear.

(8) Front panel which consists of pilot lights, switches and fuses. Fig. A.6 shows a physical layout of one module of the three phase converter. Details of mechanical drawings of the different components shown in Fig. A.6, are in [66].

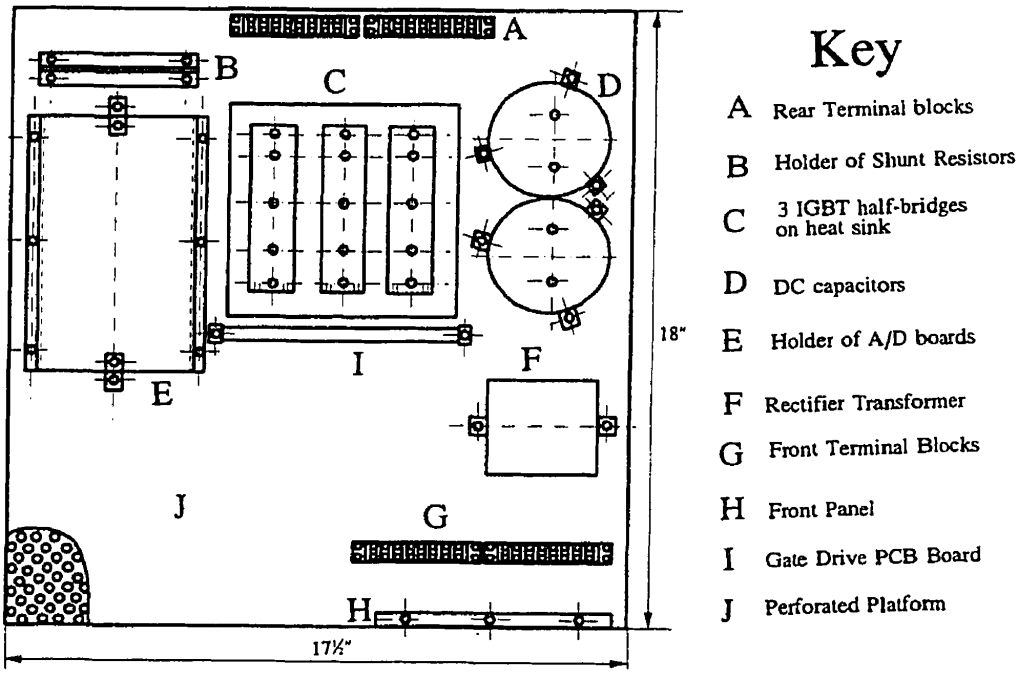


Fig. A.6: Physical layout of single module of three phase converter.

A.7 Physical Construction

The 6 modules of 3-phase converter mounted on the perforated platforms have been mounted on a standard industrial rack, with the front panels facing one side of the

rack. The 18 filter were mounted on the other side of the rack. The part number for the inductors is 195G20 from Hammond company. The filter inductors are 5.1mH and rated 20A. Mounted on the rack also is the 6-slot VME bus which carries Hydra II DSP mother board, Digital Interface Boards (with data acquisition and PWM FPGAs) and the LDG host computer. The VME bus have been positioned such that to have minimum lengths (about 1m) of the cables which carry signals to and from the converters. Fig. A.7 shows physical construction of 1 module of 3-phase converter. Fig. A.8 displays the physical construction of the overall experimental facility. Fig. A.9 shows the outline of experimental setups.

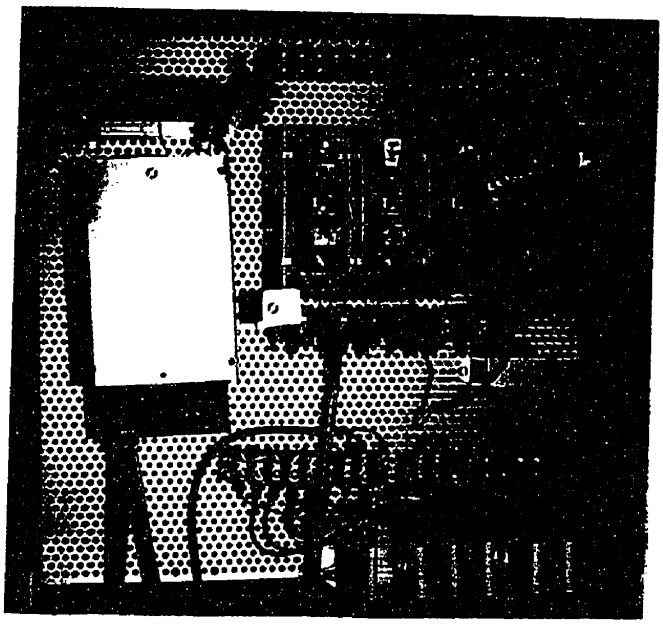


Fig. A.7: Physical construction of 1 module of 3-phase converter.

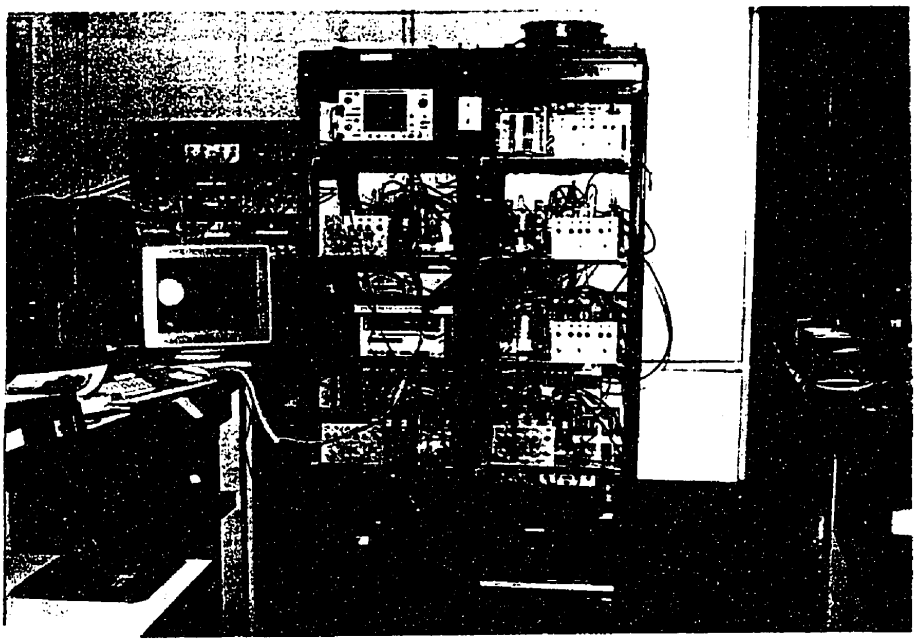


Fig. A.8: Physical construction of the overall experimental facility.

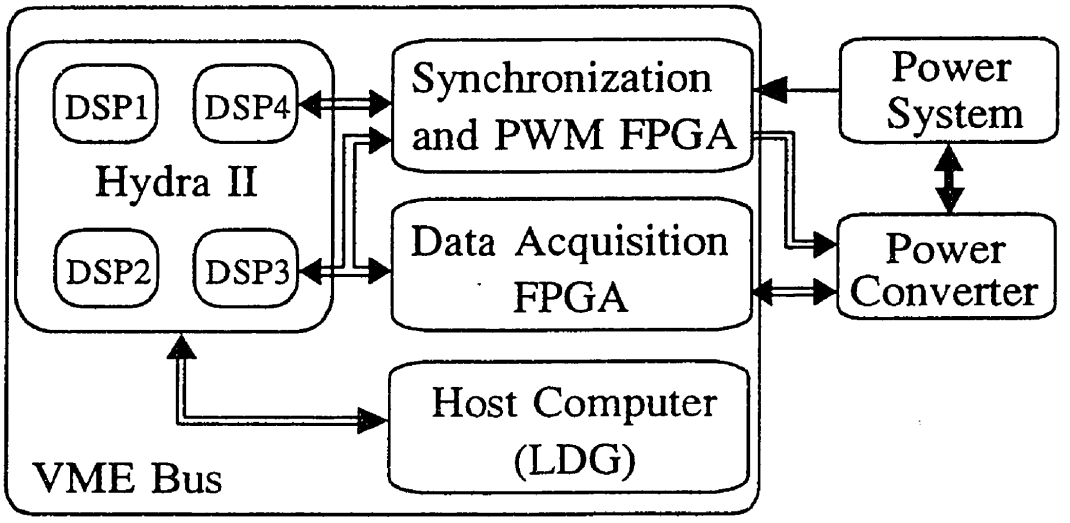


Fig. A.9: Outline of experimental setups.

APPENDIX B

ANALOG AND DIGITAL INTERFACES: ANALOG TO DIGITAL (A/D) CONVERSION AND DATA ACQUISITION

B.1 Introduction

Analog interface consists of analog signal detection, signal conditioning and analog to digital conversion. There is galvanic isolation between the power circuit and digital circuit in the data acquisition board which is provided by high speed optoisolators.

The isolated digital data are transmitted serially through line drivers to the digital interface board. On the digital interface board, there are line receivers which convert the data into standard logic and feed into the data acquisition FPGA. In the data acquisition FPGA, the serial data are converted into parallel data format ready to be read by the DSP#3 which has its expansion bus connected to the digital interface board through buffers.

The DSP#3 is also responsible to start the sampling process by giving a command to the FPGA. The FPGA in turn synthesize the sampling signal and send it to all the connected data acquisition boards through line drivers on the digital interface board and line receivers on the data acquisition boards.

The FPGA also implements Johnson counter which converts the 20MHz clock supplied by the DSP#3 to 2MHz clock required by A/D converters. The 2MHz clock is transmitted to the A/D converters through line drivers on the digital interface board and line receivers and galvanically isolated on the data acquisition boards.

B.2 Analog to Digital (A/D) Conversion

Voltage and Current signals from the power converter are scaled down within 5V peak value using potential dividers and shunt resistors respectively. The scaled signals are filtered and then converted into digital form using 16-bit serial output A/D converters. The A/D converter used is AD677 from Analog Devices company. The serial data are transmitted through optoisolators and line drivers. The A/D converters receive the sample signal and 2MHz clock from the FPGA through line receivers and optoisolators. The busy signals produced by the A/D converters go high during data conversion. The busy signals are also transmitted to the data acquisition FPGA. The falling edge of the busy signal is used to initiate an interrupt to the DSP for data acquisition. More details on data acquisition board can be found in [66].

B.2 Serial to parallel data conversion

The serial data transmitted by A/D converters are assembled in parallel by shift registers which have been implemented in the FPGA. The part number of the FPGA used for data acquisition is XC4006-4PG156C from XILINX company. There are 15 data acquisition channels. Therefore the FPGA has 15 16-bit shift registers which can be read by the DSP. The busy signals from the connected A/D converters are processed in the FPGA to initiate a hardware interrupt to the DSP#3.

Sampling is initiated by the DSP which signals the FPGA to start. The FPGA synthesize a 2μS pulse and transmit it to all the A/D converters which are connected. In this way, data conversion time remain the same regardless of the number of channels connected. The A/D converters can operate up to 100kHz sampling rate. Fig. B.1 shows

the outline of the analog and digital interface processes. More details which involve Data Acquisition, FPGA design and interface PCB board designs are given in [66].

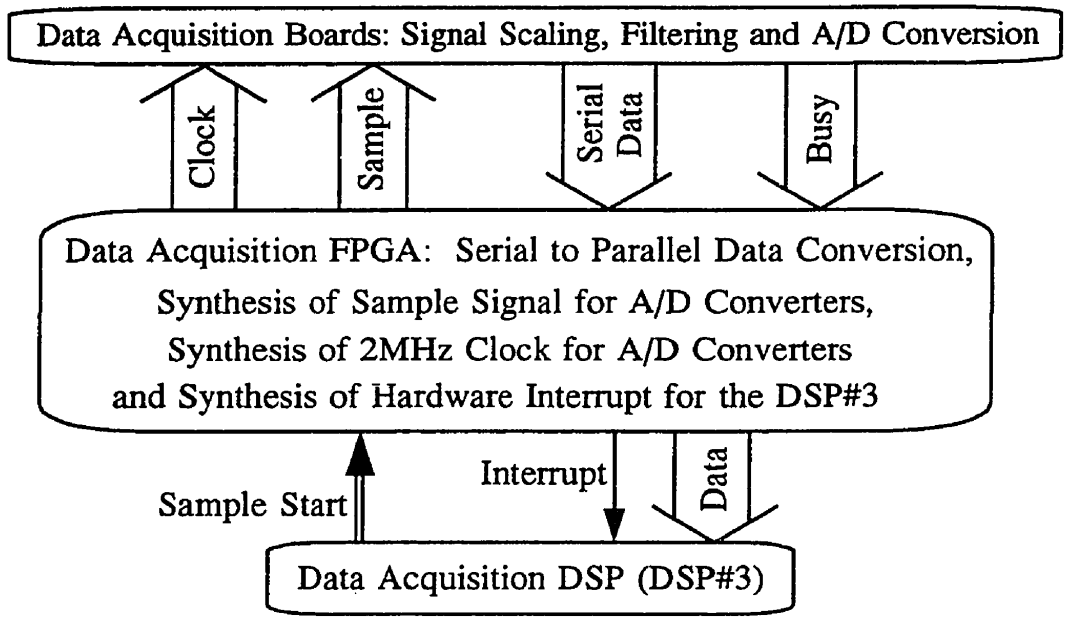


Fig. B.1: Outline of Analog and Digital Interfaces.

APPENDIX C

SYNCHRONIZATION OF THE DIGITAL SYSTEM TO THE POWER SYSTEM

C.1 Introduction

Synchronization of the digital system to power system has been done by using Phase Locked Loop (PLL). The PLL consists of Voltage Controlled Oscillator (VCO), phase difference counter, VCO counter and phase detector. The 4046 device has been used as VCO only, while the counters and phase detector have been implemented in the XILINX FPGA device, part number XC4010-4PG191. The same FPGA has been used to synthesize the switching signals for the power converters (see Appendix D).

The phase difference counter in the FPGA has 16-bit capacity and is driven by a scaled down DSP clock (20MHz). Thus the phase difference counter clock is 2.5MHz. The VCO counter in the FPGA is driven by the VCO and has a capacity of 12 bits which gives a final count of 4096. Fig. C.1 depicts the functional block diagram of the PLL. More details are given in [66].

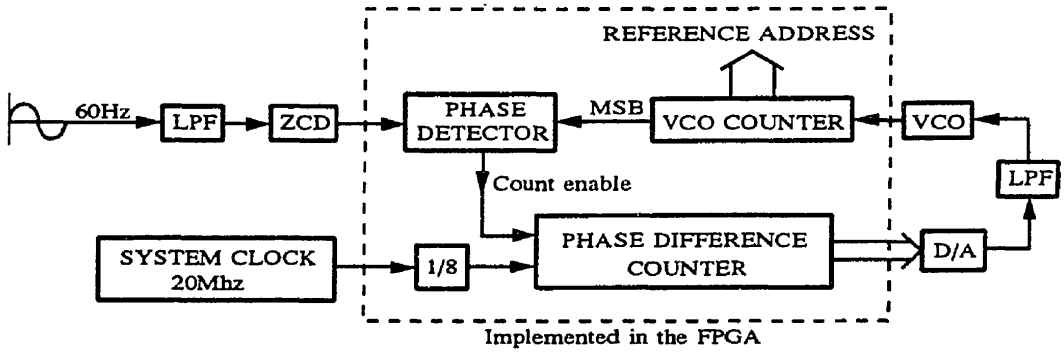


Fig. C.1: Functional block diagram of the Phase Locked Loop (PLL).

C.2 Operation of the PLL

The operation of the PLL is started by the rising edge of Zero Crossing Detector (ZCD) output, which receives the power system signal as input. The rising edge of the power system signal enables the phase different counter to start counting. The rising edge of the Most Significant Bit (MSB) of the VCO counter disables the phase difference counter from counting. The output of the phase difference counter, which is connected to a 16-data register, determines the phase difference between the power system signal and the MSB of the VCO counter.

Each time when the phase different counter is disabled from counting by MSB of VCO counter, the registered value counted is written to the 16-bit D/A converter. The writing signal of the phase difference value to the D/A converter is synthesized in the FPGA. The part number of the D/A converter used is AD669 from Analog Devices company. The output analog signal from the D/A converter is then filtered, scaled and fed to the VCO. In this way, the phase difference between the power system and the MSB of the VCO counter is kept constant if the VCO input remains constant. As a result, the power system frequency is synchronized to the Digital System clock.

C.3 Phase Modification

In order to get the phase modified, the registered output of the phase difference counter is made to be one input to a 16-bit adder. The other input to the adder is the output of a 16-bit data register which can be written directly by the DSP. In this way, the phase can be modified by writing a pre-determined value to the data register. The phase modification feature is important in order to be able to connect the power converter to the

power system at zero current, the process known as Synchronization.

C.4 Determining the address of a sampled value of the waveform (sine, cosine, etc.) or switching pattern

The maximum length of the Look Up Tables (LUT) for waveforms or switching patterns, corresponds to the final count of the 12-bit VCO counter, that is 4096 samples. At each sampling instant, the VCO counter register is read by the DSP. The number read, corresponds to the reference address of the sampled value in the LUT.

In the case of SPWM type of control, the LUT give the reference waveform which can be modified by modulation index or including feedback and/or active filtering signals. For experiments involving switching patterns, the LUT store switching commands which are written to the FPGA to synthesize the switching signals and send them to the gate drives of the power converter. There is no provision for modifying particular switching pattern in real time.

APPENDIX D

FPGA DESIGNS FOR CONTROL OF POWER CONVERTERS

D.1 Introduction

The FPGA designs for control of power converters have been accomplished using Mentor Graphics version 8 [89] and XACT version 5 [90,91] softwares on SUN computer platforms. The Mentor Graphics version 8 was used as schematic design entry and simulation tool while XACT version 5 was used to place and root the designs. The output of the XACT version 5 is of binary file format. When the binary file is loaded into the selected FPGA device, the desired digital design will be implemented.

There are different ways of loading the bitstream (binary) to the FPGA(s) [91]. Here, at McGill Power Electronics Laboratory, the DSP has been used to load the bitstream to the FPGA. The binary file format produced by the XACT version 5 software is converted into hexadecimal data array with 32-bit word length and made compatible with C-Language. The data array is included in the C-program which is compiled to run in the TMS320-C40 DSP for laoding the bitstream into the FPGAs. The DSP programs are listed in Appendix G. Loading of the FPGAs is done first before the corresponding experiment is performed.

The FPGA used for PLL and control is the XILINX device part number XC4010-4PG191 [91]. Several designs have been implemented in this FPGA, for different experiments. It was important to decide at the beginning of the hardware development, which signals to be connected to which pins. In this way, constraint files were used to ensure correct connections of signals to the FPGA pins for different designs.

In order to reduce the bulkiness of the thesis, only the schematics of the top level FPGA designs have been included in this appendix. The details have been compiled in [66].

D.2 FPGA Design for Control of 2-level 3-phase Multiconverters with Phase Shifted Triangle Carriers

For implementation of 7-Timer method described in chapter 2, the FPGA has been used to realize the hardware requirements. In order to realize carrier based regular sampling, the sampling period is determined by the carrier frequency and the number of converters to control. The sampling period is computed by the DSP and loaded into programmable period counter in the FPGA. This period counter has been designed using one 16-bit up-counter, one 16-bit magnitude comparator and one 16-bit data register. The sampling period computed by the DSP is loaded into the 16-bit data register. The output of the data register is one of the input of the magnitude comparator. The other input of the magnitude comparator is the output of the counter. The logic has been designed so that the counter is reset when its count equals the data written to the data register for sampling period.

The timers for switching ON and OFF have been realised by using 16-bit magnitude comparators, 16-bit data registers and the same counter which is used for determining sampling period. The data for switching ON and OFF calculated by the DSP are written into the data registers at the beginning of each sampling period. The switchings occur when the counter reaches the values loaded into the registers for ON and OFF timers.

Also realized in the FPGA are the demultiplexers which are used to determine

which converter will switch ON or OFF within a particular sampling period. The demultiplexers consists of data registers and decoders. The DSP determines the switching converters and loads the corresponding data to the data registers for the demultiplexers. Output of the data registers connect to the inputs of the decoder which select the corresponding converter to switch ON or OFF. The schematic of the top level FPGA design is shown in Fig. D.1.

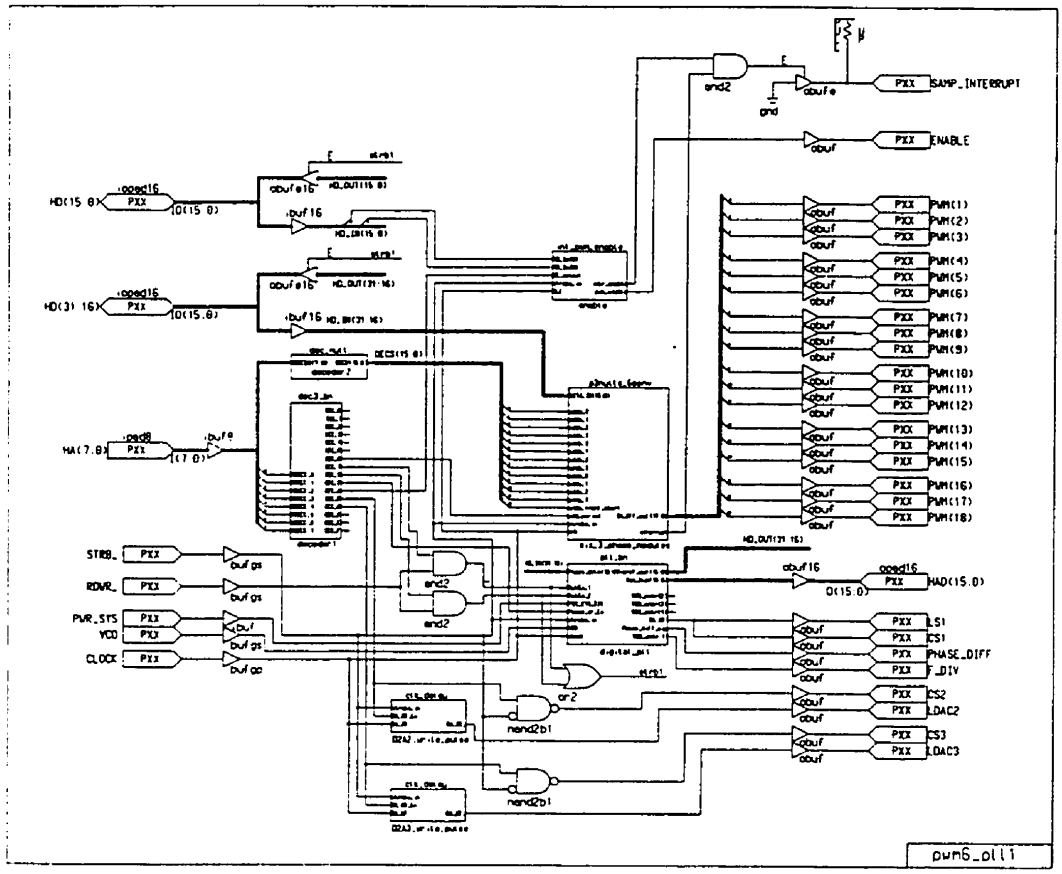


Fig. D.1: Schematic of top level FPGA design for control of 6 2-level converters with phase shifted triangle carriers.

D.3 FPGA Design for Control of 6-level 3-phase Converter under Fundamental Switching Method

In fundamental switching method, the sampling rate has to match with the pre-generated switching pattern. Five switching patterns have been used for control of 6-level converter, one for each portion in between two consecutive voltage levels. The patterns have been generated such that, each portion in between two consecutive voltage levels activate all the 3-phases (see Appendices E and G). In this way, the DSP has less number of instructions for writing the switching patterns to the FPGA.

Each pattern generated, consists of 1024 samples. Therefore the 60Hz signal can be sampled at 1024, 512, 256, etc. The FPGA design made gives a provision to choose the sampling rate from the DSP software. The sampling rates available to choose are 1024, 512, 256 or 128 per 60Hz cycle. These choices of sampling rates can be obtained by using software to enable bit 2 or 3 or 4 or 5 respectively, of the VCO counter to initiate the interrupt to the DSP.

The DSP writes to the FPGA the switching patterns of the modified addresses at the rate of the sampling rate chosen. The logic design in the FPGA processes the data written by the DSP such that to output the right signals to the right gate drives of the power converters. Fig. D.2 shows the schematic of the top level FPGA design for control of 6-level converter under fundamental switching method. The lower level designs have been compiled in [66].

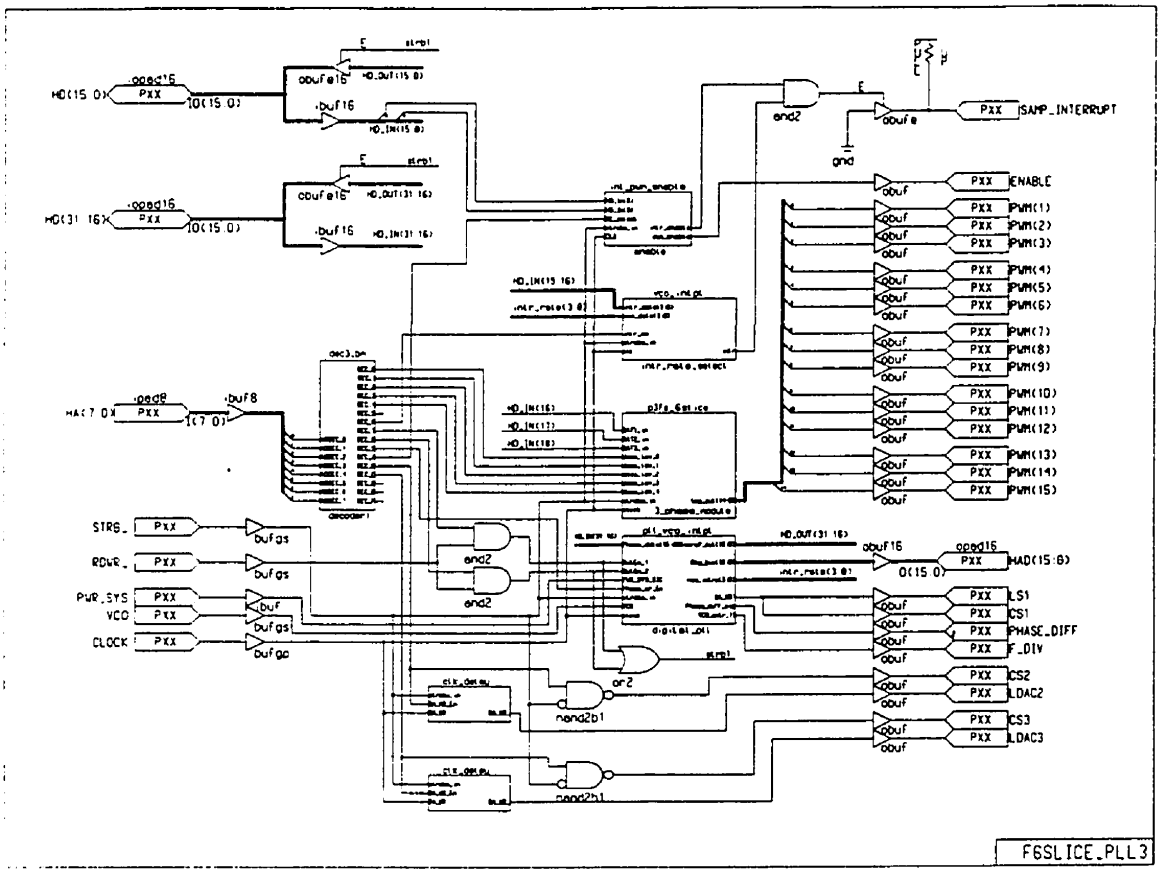


Fig. D.2: Schematic of top level FPGA design for control of 6-level converter under fundamental switching method.

D.4 FPGA Design for Control of 4-level 6-phase Converter under Fundamental Switching Method

This FPGA design has similar feature as that of Appendix D.3. The only difference is that, in this case only three switching patterns are required instead of five (see Appendices E.3 and G.5). The three switching patterns have been generated such that

the switchings of the positive and negative converters for all 3-phases are correctly effected. The choice of sampling rate is done the same way as for control of 6-level converter described in section D.3. The FPGA top level design for control of 2 4-level converters operated in 6-phase mode is shown in Fig. D.3.

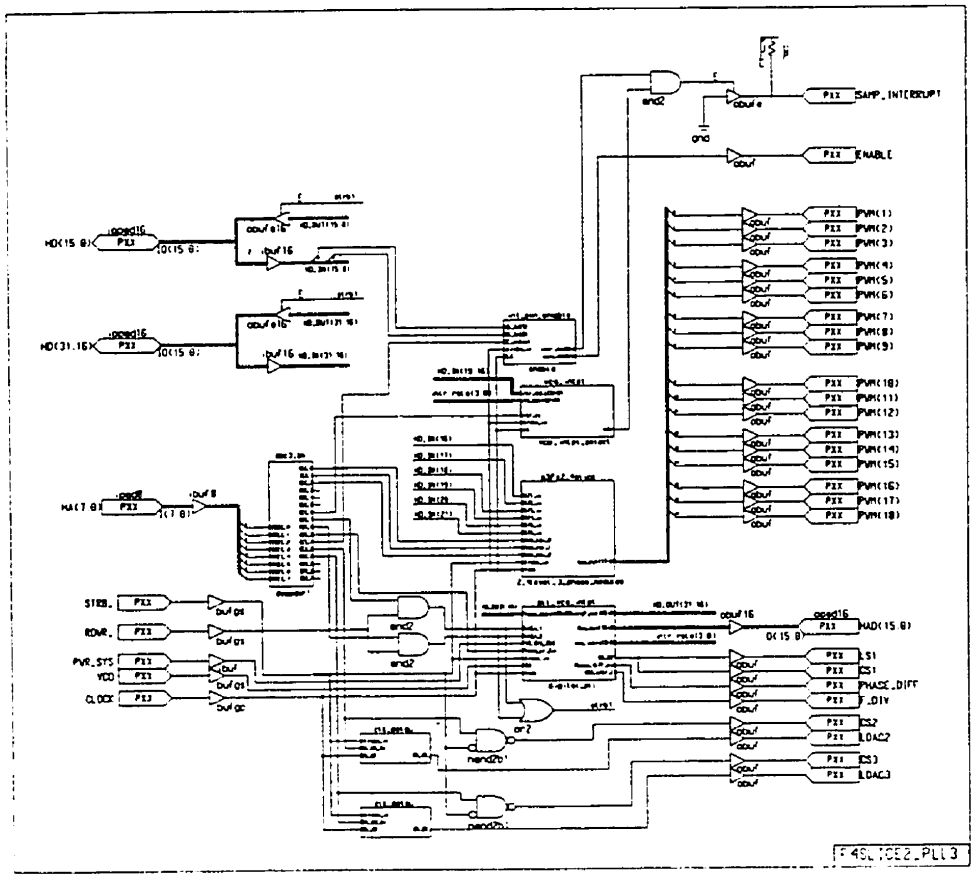


Fig. D.3: Schematic of top level FPGA design for control of 2 4-level converters in 6-phase mode under fundamental switching method.

APPENDIX E

GENERATION OF SWITCHING PATTERNS

E.1 Introduction

In the experiments involving multilevel converters, fundamental switching method was used. In fundamental switching method of multilevel converters, one has some degrees of freedom to decide on the harmonic content and/magnitude of the output voltage [42,63,64,85]. Each switching angle gives one degree of freedom.

For 6-level converter used in this thesis, there are two switching angles and hence gives only two degrees of freedoms which were used to eliminate the 5^{th} and the 7^{th} harmonics in the output voltage.

For 4-level converters which were employed to implement 6-phase STATCOM, only one degree of freedom is available. This was used to eliminate the 5^{th} harmonic for both the positive converter and the negative converter.

The switching patterns have been generated in such a way that the DSP processor will have least number of instructions to execute, at the same time, be able to implement total dc voltage regulation and individual dc capacitor voltage equalization. The task of the DSP processor in each interrupt, is to read the reference address, modify according to the control law and finally use the modified address to read the corresponding switching pattern and write to the FPGA. In the FPGA, the current switching pattern written by the DSP is processed to give the corresponding switching signals to the multilevel converter(s). It is therefore very important to ensure compatibility between the switching pattern, DSP program and FPGA design for a particular experiment.

E.2 Switching Pattern for 6-level 3-phase Converter under Fundamental Switching Method with elimination of 5th and 7th Harmonics

One cycle of the 6-level voltage waveform is shown in Fig. E.1. The switching angles α_1 and α_2 are chosen to eliminate the 5th and 7th harmonics.

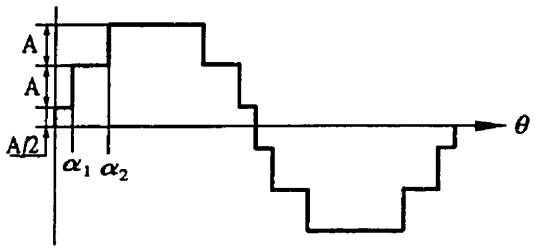


Fig. E.1: 6-level voltage waveform.

Applying Fourier Series analysis to the voltage waveform of Fig. E.1, it can be deduced that the Fourier series coefficients, b_n, are given by

$$b_n = \frac{2A}{n\pi}\{1 + 2Cos(n\alpha_1) + 2Cos(n\alpha_2)\}, \qquad n = 1, 3, 5, 7, 9, \ldots . \tag{E.1}$$

For 3-phase systems with open wye or delta connection, all the harmonics which are multiples of 3 cancel out. In order to eliminate the 5th and 7th harmonics, then the Fourier coefficients b5 and b7 in (E.1) are set to zero as given in (E.2).

$$\begin{aligned} 1 + 2Cos(5\alpha_1) + 2Cos(5\alpha_2) &= 0 \\ 1 + 2Cos(7\alpha_1) + 2Cos(7\alpha_2) &= 0 \end{aligned} \tag{E.2}$$

Equation (E.2) is nonlinear transcendental equation which can be solved by the Newton-Raphson method. Using MATLAB package [65], the angles are α_1 = 12.285° and α_2 = 33.6087°. These switching angles were used in a C-Language program to generate one cycle of the switching patterns for the five blocks of the 6-level voltage waveform. The switching pattern for each block contains 1024, 3-bit data points (1 or 0), 1 bit for each phase. The five switching patterns have been stored in five separate files which are included in the DSP program for control of 6-level converter. Details of control of

multilevel converters with fundamental switching method are given in chapter V and [63,66,82,85]. The list of the C-Language program used to generate switching patterns for control of 6-level converter is given in Table E.1. The program has been developed using Borland C++ version 2.0 programming environment [92,93].

Table E.1: Program list for generation of switching patterns for control of 6-level converter under fundamental switching method with elimination of 5^{th} and 7^{th} harmonics.

```
/*************************************************/
Program six_lev.cpp. Data file: inpt
/*************************************************/
/* This is data file "inpt" which is read by the program to
initialize some of the constants
**************************************************
1 1024 500 12195 3 2 10 140 0.000125 150 150 31 0.001
0.04 0.0 3 75.0
**************************************************
*/
#include <stdio.h>
#include <dos.h>
#include <stdlib.h>
#include <math.h>
#include <graphics.h>
#include <conio.h>
#define pi 4*atan(1)
#define STOP 's'

main (void)
{
setcbrk(1);
char ch;
static long dl1, dl2, dl3, dl4, dl5;
static long Dl1[5], Tabx[3][5];
static int gmode, errorcode, gdriver = DETECT;
static int n1, Nk, Nk3;
static int xmax, ymax, xmax1, col, tNk, tNk1, Nk31;
static int i, j, count, linelength;
static float f, kf, kt, kc, ki, kph, ph1, sine1, sine2;
static float tabv[3], tabx[3][5], Sw[3], S1[26], S[26];
static float Ss1[26], Ss[26], ts1[26], ts[26];
static float Vm[3], Vpwm1[3], Vpwm[3], Cnk[26];
static float ns, n, no1, mx, im, im1, ic, ic1, it1, it, l, R;
static float w, Vma, Vma1, Vdc, Ac, Va, Vp1, Vp, Vk;
static float C, Ck, Ctk, Vms1, Vms, Vmc1, Vmc, Vmb1, Vmb;
static float Ndk, Ndk1, Nd, k3;
static float w1, m1, Vb, Vc, Vpk1, Vpk, Vps1, Vps;
static float ica, icb, icc, icd, ice;
static float m, dt, E, iac, me;
static float stk, st, t, t1, t2;
static float tc, tw, Tm, tm, dtl;
FILE *inpt;
if ((inpt = fopen("inpt", "r")) == NULL)
{
fprintf(stderr, "Cannot open input data file.\n");
        printf("\n");
        printf("Press any key to return:");
        getch();
        return (1);
}
fscanf(inpt,"%g %g %g %d %d %g %g %g %g %g %g %g
%g %g %g %g",
&kf,&kt,&kc,&n1,&col,&Nd,&ki,&m,&k3,&Vdc,&Ac,&no1,&
l,&R,&kph,&Ndk);
FILE *out1;
FILE *out2;
FILE *out3;
FILE *out4;
FILE *out5;
if ((out1 = fopen("dat1.h", "wt+")) == NULL)
{
fprintf(stderr, "Cannot open output data file1.\n");
printf("\n");
printf("Press any key to return:");
getch();
return 1;
}
if ((out2 = fopen("dat2.h", "wt+")) == NULL)
{
fprintf(stderr, "Cannot open output data file2.\n");
printf("\n");
printf("Press any key to return:");
getch();
return 1;
}
if ((out3 = fopen("dat3.h", "wt+")) == NULL)
{
fprintf(stderr, "Cannot open output data file3.\n");
printf("\n");
printf("Press any key to return:");
getch();
return 1;
}
if ((out4 = fopen("dat4.h", "wt+")) == NULL)
{
fprintf(stderr, "Cannot open output data file4.\n");
printf("\n");
```

```
printf("Press any key to return:");
getch();
return 1;
}
if ((out5 = fopen("dat5.h", "wt+")) == NULL)
{
fprintf(stderr, "Cannot open output data file5.\n");
printf("\n");
printf("Press any key to return:");
getch();
return 1;
}
fprintf(out1,"static unsigned int tablex1[] = {");
fprintf(out2,"static unsigned int tablex2[] = {");
fprintf(out3,"static unsigned int tablex3[] = {");
fprintf(out4,"static unsigned int tablex4[] = {");
fprintf(out5,"static unsigned int tablex5[] = {");
count = 1;
Nk = ceil(Ndk); tNk = 2*Nk; tNk1 = tNk+1;
/*
Request autodetection. Initialize graphics.
The "Borland Graphics Initialization" (BGI) file are normally
located in ..\GBI subdirectory. They can also be copied to the
working subdirectory.
*/
initgraph(&gdriver, &gmode," ");
/* read result of initialization */
errorcode = graphresult();
if (errorcode != grOk)  /* an error occured */
{
        printf("Graphics error: %s\n",
grapherrormsg(errorcode));
        printf("\n");
        printf("Press any key to halt:");
        getch();
        exit(1);
}
f = 60;
w = 2*pi*f;
w1 = w;
ph1 = kph*pi/2;
sine1 = sin(2*pi*(12.285/360));
sine2 = sin(2*pi*(33.6087/360));
m1 = m;
me = 100;
Tm = 1.0/f;
Nk3 = Nk*2 - 1; Nk31 = Nk3 + 1;
dt = 1.0/(kf*f*kt);
t = 0; t1 = 0; t2 = 0;
Ck = 2*Vdc/Nk3;
for (j=0; j<Nk31; j++)
{
Cnk[j] = Vdc - j*Ck;
}
dt1 = dt/1;
Vk = Vdc;
xmax = getmaxx();
ymax = getmaxy();
xmax1 = no1*xmax;
line(0,0, xmax,0);
line(xmax,0, xmax,ymax);
line(xmax,ymax, 0,ymax);
line(0,ymax, 0,0);
setbkcolor(co1);
//while (t <= 30)
while(!kbhit())
        {
n = n1*t2;
ns = n1*t1;
mx = n1*t;
for(i=0; i<3; i++)
        {
        Sw[i] = sin(w1*t - (i*2*pi/3));
        Vm[i] = m1*Sw[i];
        }
                E = me*sin(w1*t + ph1);
                Vma = m1*sin(w1*t + ph1);
for(i=0; i<3; i++)
        {
        if(Sw[i] > sine2)
        {
        Vpwm[i] = Cnk[0];
        tabv[i] = 31.0;
        tabx[i][0] = 1.0;
        tabx[i][1] = 1.0;
        tabx[i][2] = 1.0;
        tabx[i][3] = 1.0;
        tabx[i][4] = 1.0;
        }
        if((Sw[i] > sine1) && (Sw[i] < sine2))
        {
        Vpwm[i] = Cnk[1];
        tabv[i] = 30.0;
        tabx[i][0] = 0.0;
        tabx[i][1] = 1.0;
        tabx[i][2] = 1.0;
        tabx[i][3] = 1.0;
        tabx[i][4] = 1.0;
        }
        if((Sw[i] < sine1) && (Sw[i] > 0))
        {
        Vpwm[i] = Cnk[2];
        tabv[i] = 28.0;
        tabx[i][0] = 0.0;
        tabx[i][1] = 0.0;
        tabx[i][2] = 1.0;
        tabx[i][3] = 1.0;
        tabx[i][4] = 1.0;
        }
        if((Sw[i] < 0) && (Sw[i]> -sine1))
        {
        Vpwm[i] = Cnk[3];
        tabv[i] = 24.0;
        tabx[i][0] = 0.0;
        tabx[i][1] = 0.0;
        tabx[i][2] = 0.0;
        tabx[i][3] = 1.0;
        tabx[i][4] = 1.0;
        }
        if((Sw[i] < -sine1) && (Sw[i] > -sine2))
        {
        Vpwm[i] = Cnk[4];
        tabv[i] = 16.0;
        tabx[i][0] = 0.0;
        tabx[i][1] = 0.0;
        tabx[i][2] = 0.0;
        tabx[i][3] = 0.0;
        tabx[i][4] = 1.0;
```

```
            }
            if(Sw[i] < -sine2)
            {
            Vpwm[i] = Cnk[5];
            tabv[i] = 0.0;
            tabx[i][0] = 0.0;
            tabx[i][1] = 0.0;
            tabx[i][2] = 0.0;
            tabx[i][3] = 0.0;
            tabx[i][4] = 0.0;
            }
            }
                        im = im + (Vma - R*im)*dtl;

iac = iac + (E - Vpk - R*iac)*dtl;
                        if (mx >= xmax)
                        {
                                    ica = ica + (S[0] - R*ica)*dtl;
                                    icb = icb + (S[1] - R*icb)*dtl;
                                    icc = icc + (S[2] - R*icc)*dtl;
                                    it =  it + (Vp - R*it)*dtl;
                        }
                        Va = S[0];
                        Vb = S[1];
                        Vc = S[2];
                        ic = ica;
            if (n >= xmax)
                                    {
                                    ch = getch();
                                    if (ch == STOP)
{
fclose(inpt);
closegraph();
exit(1);
}
cleardevice();
t1 = 0;
t2 = 0;
line(0,0, xmax,0);
line(xmax,0, xmax,ymax);
line(xmax,ymax, 0,ymax);
line(0,ymax, 0,0);
}
if (mx >= xmax1)
{
if (tw >= tc)
{
tw = 0;
}
for(j = 0; j < 5; j++)
{
for(i = 0; i < 3; i++)
{
Tabx[i][j] = (int)(tabx[i][j]);
Tabx[i][j] = (Tabx[i][j]) << (16 + i );
}
Dl1[j] = Tabx[0][j] | Tabx[1][j] | Tabx[2][j];
}
fprintf(out1, "0x%lx", Dl1[0]);
fprintf(out2, "0x%lx", Dl1[1]);
fprintf(out3, "0x%lx", Dl1[2]);
fprintf(out4, "0x%lx", Dl1[3]);
fprintf(out5, "0x%lx", Dl1[4]);
if(count == int(kt))
{
fprintf(out1," };");
fclose(out1);
fprintf(out2," };");
fclose(out2);
fprintf(out3," };");
fclose(out3);
fprintf(out4," };");
fclose(out4);
fprintf(out5," };");
fclose(out5);
}
count = count + 1;
linelength = linelength + 1;
if(linelength%8 == 0)
{
fprintf(out1,",\n");
fprintf(out2,",\n");
fprintf(out3,",\n");
fprintf(out4,",\n");
fprintf(out5,",\n");
}
else
{
fprintf(out1,", ");
fprintf(out2,", ");
fprintf(out3,", ");
fprintf(out4,", ");
fprintf(out5,", ");
}
}
putpixel(n, (ymax*.1)-int(Vma/4), 4);
for(i=0; i<3; i++)
{
if (Vpwm[i] != Vpwm1[i])
{
line(int(n), (ymax*(0.3 + 0.2*i))-int(Vpwm1[i]/4), int(n),
(ymax*(0.3 + 0.2*i))-int(Vpwm[i]/4));
Vpwm1[i] = Vpwm[i];
}
else line(int(ns), (ymax*(0.3 + 0.2*i))-int(Vpwm1[i]/4), int(n),
(ymax*(0.3 + 0.2*i))-int(Vpwm[i]/4));
line(0,(ymax*(0.3 + 0.2*i)), xmax,(ymax*(0.3 + 0.2*i)));
}
tm = tm + dt;
t1 = t2;
t2 = t2 + dt;
t = t + dt;
tw = tw + dt;
Vma1 = Vma;
Vp1 = Vp;
Vp = 0;
Vps1 = Vps;
Vps = 0;
}
fclose(inpt);
//fclose(out);
getch();
closegraph();
return 0;
}
```

E.3 Switching Pattern for 4-level 6-phase Converter under Fundamental Switching Method with elimination of 5th Harmonic

Fig. E.2 shows one cycle of the 4-level voltage waveforms for 6-phase operation. The switching angles α is chosen to eliminate the 5th harmonic. Applying Fourier Series analysis to the voltage waveform of Fig. E.2(a), to obtain the Fourier series coefficients, yields

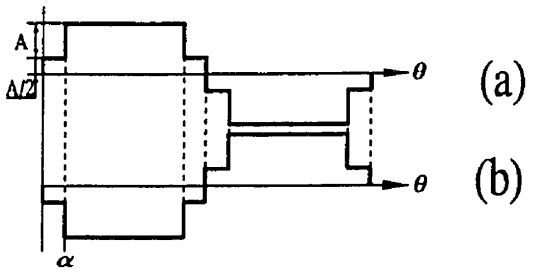


Fig. E.2: 4-level voltage waveforms for 6-phase operation. (a) Waveform for positive converter. (b) Waveform for negative converter.

$$b_n = \frac{2A}{n\pi}\{1 + 2Cos(n\alpha)\}, \qquad n = 1, 3, 5, 7, 9, \ldots . \tag{E.3}$$

The Fourier coefficients for the voltage waveform of Fig. E.2(b) have the same magnitude as those for Fig. E.2(a) but 180° out of phase.

As mentioned in section E.2, for 3-phase systems with open wye or delta connection, all the harmonics which are multiples of 3 cancel out. In order to eliminate the 5th harmonic, then the Fourier coefficients b5 in (E.3) is set to zero as given in (E.4).

$$1 + 2Cos(5\alpha) = 0 \tag{E.4}$$

The solution for (E.4) is α = 24.0°. This switching angle was used in a C-Language program to generate one cycle of the switching patterns for the three blocks of the 4-level 6-phase voltage waveforms. The switching pattern for each block contains 1024, 6-bit data points (1 or 0), 2 bits for each phase (1-bit for positive and 1-bit for negative). The three switching patterns have been stored in three separate files which are included in the DSP program for control of 4-level 6-phase converter. Details of control

of multilevel converters with fundamental switching method are given in chapter V, chapter VI and [42,63,82,85]. The list of the C-Language program used to generate switching patterns for control of 4-level 6-phase converter is given in Table E.2. The program has been developed using Borland C++ version 2.0 programming environment [92,93].

Table E.2: Program list for generation of switching patterns for control of 4-level 6-phase converter operated under fundamental switching method with elimination of 5th harmonics.

```
/*****************************************/
Program six_ph.cpp. Data file: inpt
/*****************************************/

/* This is data file "inpt" which is read by the program to
intialize some of the constants
*****************************************************
1 1024 500 12195 3 2 10 140 0.000125 150 150 31 0.001 0.04
0.0 2 75.0
*****************************************************
*/

#include <stdio.h>
#include <dos.h>
#include <stdlib.h>
#include <math.h>
#include <graphics.h>
#include <conio.h>
#define pi 4*atan(1)
#define STOP 's'

main (void)
{
setcbrk(1);
char ch;
static long dl1, dl2, dl3, dl4, dl5;
static long Dl1[5], Tabx[3][5];
static int gmode, errorcode, gdriver = DETECT;
static int n1, Nk, Nk3;
static int xmax, ymax, xmax1, col, tNk, tNk1, Nk31;
static int i, j, count, linelength;
static float f, kf, kt, kc, ki, kph, ph1, sine1, sine2;
static float tabv[3], tabx[3][5], Sw[3], Swsh[3], S1[26], S[26];
static float Ss1[26], Ss[26], ts1[26], ts[26];
static float Vm[3], Vpwm1[3], Vpwm[3], Vpwmsh[3], Cnk[26];
static float Vpwmsh1[3], Vpwmsh[3], Vpwmtot1[3], Vpwmtot[3];
static float ns, n, no1, mx, im, im1, ic, ic1, it1, it, l, R;
static float w, Vma, Vma1, Vdc, Ac, Va, Vp1, Vp, Vk;
static float C, Ck, Ctk, Vms1, Vms, Vmc1, Vmc, Vmb1, Vmb;
static float Ndk, Ndk1, Nd, k3, phsw;
static float w1, m1, Vb, Vc, Vpk1, Vpk, Vps1, Vps;
static float ica, icb, icc, icd, ice;
static float m, dt, E, iac, me;
static float stk, st, t, t1, t2;
static float tc, tw, Tm, tm, dtl;
FILE *inpt;
if ((inpt = fopen("inpt", "r")) == NULL)
{
fprintf(stderr, "Cannot open input data file.\n");
printf("\n");
printf("Press any key to return:");
getch();
return (1);
}
fscanf(inpt,"%g %g %g %d %d %g %g %g %g %g %g %g %g %g %g %g",
&kf,&kt,&kc,&n1,&col,&Nd,&ki, &m,&k3,&Vdc,&Ac,&no 1,&
l,&R,&kph,&Ndk,&phsw);
FILE *out1;
FILE *out2;
FILE *out3;
if ((out1 = fopen("dat1.h", "wt+")) == NULL)
{
fprintf(stderr, "Cannot open output data file1.\n");
printf("\n");
printf("Press any key to return:");
getch();
return 1;
}
if ((out2 = fopen("dat2.h", "wt+")) == NULL)
{
fprintf(stderr, "Cannot open output data file2.\n");
printf("\n");
printf("Press any key to return:");
getch();
return 1;
}
if ((out3 = fopen("dat3.h", "wt+")) == NULL)
{
fprintf(stderr, "Cannot open output data file3.\n");
printf("\n");
printf("Press any key to return:");
```

```
getch();
return 1;
}
fprintf(out1,"static unsigned int tablex1[] = {");
fprintf(out2,"static unsigned int tablex2[] = {");
fprintf(out3,"static unsigned int tablex3[] = {");
count = 1;
Nk = ceil(Ndk); tNk = 2*Nk; tNk1 = tNk+1;
/*
Request autodetection. Initialize graphics.
The "Borland Graphics Initialization" (BGI) file are normally
located in ..\GBI subdirectory. They can also be copied to the
working subdirectory.
*/
initgraph(&gdriver, &gmode," ");
/* read result of initialization */
errorcode = graphresult();
if (errorcode != grOk)  /* an error occured */
{
printf("Graphics error: %s\n", grapherrormsg(errorcode));
printf("\n");
printf("Press any key to halt:");
getch();
exit(1);
}
f = 60;
w = 2*pi*f;
w1 = w;
ph1 = kph*pi/2;
sine1 = sin(2*pi*(24/360));
m1 = m;
me = 100;
Tm = 1.0/f;
Nk3 = Nk*2 - 1; Nk31 = Nk3 + 1;
dt = 1.0/(kf*f*kt);
t = 0; t1 = 0; t2 = 0;
Ck = 2*Vdc/Nk3;
for (j=0; j<Nk31; j++)
{
Cnk[j] = Vdc - j*Ck;
}
dtl = dt/l;
Vk = Vdc;
xmax = getmaxx();
ymax = getmaxy();
xmax1 = no1*xmax;
line(0,0, xmax,0);
line(xmax,0, xmax,ymax);
line(xmax,ymax, 0,ymax);
line(0,ymax, 0,0);
setbkcolor(col);
//while (t <= 30)
while(!kbhit())
{
n = n1*t2;
ns = n1*t1;
mx = n1*t;
for(i=0; i<3; i++)
{
Sw[i] = sin(w1*t - (i*2*pi/3));
Swsh[i] = Sw[i];
Vm[i] = m1*Sw[i];
}
E = me*sin(w1*t + ph1);
Vma = m1*sin(w1*t + ph1);
for(i=0; i<3; i++)
{
if(Sw[i] > sine1)
{
Vpwm[i] = Cnk[0];
tabx[i][0] = 1.0;
tabx[i][1] = 1.0;
tabx[i][2] = 1.0;
}
if(Swsh[i] > sine1) Vpwmsh[i] = Cnk[3];
if((Sw[i] > 0) && (Sw[i] < sine1))
{
Vpwm[i] = Cnk[1];
tabx[i][0] = 0.0;
tabx[i][1] = 1.0;
tabx[i][2] = 3.0;
}
if((Swsh[i] > 0) && (Swsh[i] < sine1)) Vpwmsh[i] = Cnk[2];
if((Sw[i] < 0) && (Sw[i] > -sine1))
{
Vpwm[i] = Cnk[2];
tabx[i][0] = 0.0;
tabx[i][1] = 2.0;
tabx[i][2] = 3.0;
}
if((Swsh[i] < 0) && (Swsh[i] > -sine1)) Vpwmsh[i] = Cnk[1];
if(Sw[i] < -sine1)
{
Vpwm[i] = Cnk[3];
tabx[i][0] = 2.0;
tabx[i][1] = 2.0;
tabx[i][2] = 2.0;
}
if(Swsh[i] < -sine1) Vpwmsh[i] = Cnk[0];
Vpwmtot[i] = (Vpwm[i] + Vpwmsh[i])/2;
}
im = im + (Vma - R*im)*dtl;
iac = iac + (E - Vpk - R*iac)*dtl;
if (mx >= xmax)
{
ica = ica + (S[0] - R*ica)*dtl;
icb = icb + (S[1] - R*icb)*dtl;
icc = icc + (S[2] - R*icc)*dtl;
it =  it + (Vp - R*it)*dtl;
}
Va = S[0];
Vb = S[1];
Vc = S[2];
ic = ica;
if (n >= xmax)
{
ch = getch();
if (ch == STOP)
{
fclose(inpt);
closegraph();
exit(1);
}
cleardevice();
t1 = 0;
t2 = 0;
line(0,0, xmax,0);
line(xmax,0, xmax,ymax);
```

```
line(xmax,ymax, 0,ymax);
line(0,ymax, 0,0);
}
if (mx >= xmax1)
{
if (tw >= tc)
{
tw = 0;
}
for(j = 0; j < 3; j++)
{
for(i = 0; i < 3; i++)
{
Tabx[i][j] = (int)(tabx[i][j]);
Tabx[i][j] = (Tabx[i][j]) << (16 + (2*i));
}
Dl1[j] = Tabx[0][j] | Tabx[1][j] | Tabx[2][j];
}
fprintf(out1, "0x%lx", Dl1[0]);
fprintf(out2, "0x%lx", Dl1[1]);
fprintf(out3, "0x%lx", Dl1[2]);
if(count == int(kt))
{
fprintf(out1," };");
fclose(out1);
fprintf(out2," };");
fclose(out2);
fprintf(out3," };");
fclose(out3);
}
count = count + 1;
linelength = linelength + 1;
if(linelength%8 == 0)
{
fprintf(out1,",\n");
fprintf(out2,",\n");
fprintf(out3,",\n");
}
else
{
fprintf(out1,", ");
fprintf(out2,", ");
fprintf(out3,", ");
}
}
putpixel(n, (ymax*.1)-int(Vma/4), 4);
line(0,(ymax*(0.1)), xmax,(ymax*(0.1)));
for(i=0; i<3; i++)
{
if (Vpwm[i] != Vpwm1[i])
{
line(int(n), (ymax*(0.3 + 0.2*i))-int(Vpwm1[i]/8), int(n),
(ymax*(0.3 + 0.2*i))-int(Vpwm[i]/8));
Vpwm1[i] = Vpwm[i];
}
else line(int(ns), (ymax*(0.3 + 0.2*i))-int(Vpwm1[i]/8), int(n),
(ymax*(0.3 + 0.2*i))-int(Vpwm[i]/8));
line(0,(ymax*(0.3 + 0.2*i)), xmax,(ymax*(0.3 + 0.2*i)));
if (Vpwmsh[i] != Vpwmsh1[i])
{
line(int(n), (ymax*(0.4 + 0.2*i))-int(Vpwmsh1[i]/8), int(n),
(ymax*(0.4 + 0.2*i))-int(Vpwmsh[i]/8));
Vpwmsh1[i] = Vpwmsh[i];
}
else line(int(ns), (ymax*(0.4 + 0.2*i))-int(Vpwmsh1[i]/8), int(n),
(ymax*(0.4 + 0.2*i))-int(Vpwmsh[i]/8));
line(0,(ymax*(0.4 + 0.2*i)), xmax,(ymax*(0.4 + 0.2*i)));
}
tm = tm + dt;
t1 = t2;
t2 = t2 + dt;
t = t + dt;
tw = tw + dt;
Vma1 = Vma;
Vp1 = Vp;
Vp = 0;
Vps1 = Vps;
Vps = 0;
}
fclose(inpt);
//fclose(out);
getch();
closegraph();
return 0;

}
```

APPENDIX F

ORGANIZATION OF SIMULATION PROGRAMS

The programs used for simulations of power electronics systems presented in this thesis have been developed in Borland C++ version 2.0 programming environment. The C++ feature available in the Borland C++ programming environment was not utilised. Instead, the standard C-Language feature have been used to develop the simulation programs.

The simulation programs have been used for different purposes:

(1) Where experimental setup is possible, the simulation results have been used as a quick check for a planned experimental setup.

(2) Where experimental setup is not possible due to inadequacy of the experimental facilities, for example in chapters 3, 4 and 5, only simulation programs have been used to study the power electronic system.

It has to be admitted that the simulation programs developed are not in standard format compared to the existing commercial simulation softwares such as PSpice, PSCAD, etc. The objectives of developing the simulation programs instead of using the existing commercial softwares are:

(1) To develop programming skills in C-Language so that to be acquainted in real-time programming for control using Digital Signal Processors (DSP). For example, in chapter 2, the algorithm for 7-Timer method developed in the simulation program has been ported into the DSP program.

(2) To have full control of the program. For example, the execution of the programs

can be interrupted any time, while most of the commercial simulation softwares can not be interrupted.

(3) To learn how to develop the differential equations of the power electronics system from first principles.

The programs developed for simulations of different systems have the following common features:

(1) The program can display the selected variables immediately after computation in order to monitor closely the validity of the results.

(2) The program can be interrupted any time in order not to continue with wrong results caused by wrong data or wrong formulation.

(3) For the variables which require frequent changes, data files have been used which can be read by the simulation program. The changes can be made in the data files without making any changes in the source code of the simulation program. This feature avoids re-compilation of the source program.

(4) On request, the selected values of the variables computed can be saved in a file for further analysis such as Fast Fourier Transform (FFT).

Fig. F.1 shows the simplified flow chart of the simulation programs used in studying power electronics systems presented in this thesis. The listings of the source programs are not included in order to reduce the size of the thesis.

In all the simulation programs, the Euler Method [94] of integration has been used. This method of integration is not very accurate and may become unstable when coarse integration step is used. This fact had been taken into account throughout the simulation studies and remedied by using as fine the integration step as required. The

reason why the Euler Method of integration has been used is that, it was not the purpose of this thesis work to perform precise computation in the simulation studies. Rather, the simulation studies aimed at testing the ideas which have been developed by simulation, then when possible, implement the ideas experimentally. On the other hand, in the experimental setups, the signals are sampled at relatively low rate resulting in less accuracy. Therefore it was not stringent to employ integration method such as Runge-Kutta [94] which is very accurate but slow.

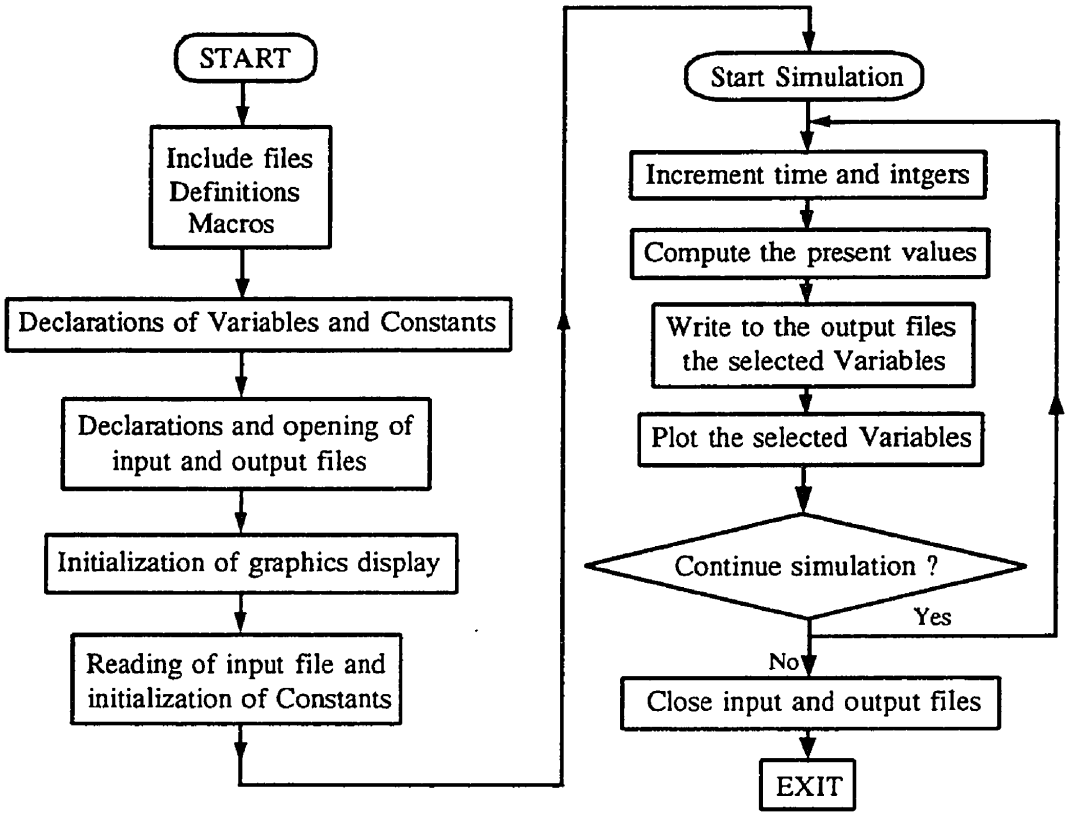


Fig. F.1: Simplified Flow Chart for Simulation Programs (Developed in C-Code).

APPENDIX G

SOFTWARES FOR DSPs

G.1 Introduction

The softwares for the DSPs were developed using LDG host computer [95,96] and Borland C++ version 2.0 programming environment [92,93]. All the DSP programs were developed in C-Language [97]. The C-Language programs were compiled and linked to get executables for the DSPs, using Optimizing C compiler [97] which is included in the purchase of the Hydra II DSP motherboard [98,99].

In Hydra II DSP motherboard, two DSPs have been used for real time control of power converters, DSP3 and DSP4. These two DSPs have their expansion buses accessible directly. The two DSPs have been made to run in synchronism. The DSP3 has been used for data acquisition and DSP4 has been used to perform control algorithms. The two DSPs have been made to communicate to each other through their 8-bit COM PORTS.

G.2 DSP Program list for loading the configuration bitstream to the FPGAs

The configuration bitstream is loaded to the two FPGAs in Slave Serial Mode [91] using DSP3. The C-Language program used is shown in Table G.1. The loading of the configuration bitstream into the FPGAs is performed just after the system is powered.

Table G.1: Program list for DSP3 to load the configuration bitstream to the FPGAs.

```
*****************************************************
/* Program FPGA.C, located in c:\hydra\..\source for all
experimental setups */
*****************************************************
#include "hydra.h"
#include "bits.h" /* File containing configuration bitstream in
hexadecimal format */
#include "H_II_map.h" /* Definition of physical addresses */
main() {
int i,j;
for (i=0;i<=sizeof(bits)/sizeof(bits[0]); i++)
        {
                for (j=0; j<=31; j++)
                *(expansion)=bits[i] << j;
                }
/* now wait a bit */
for (i-0; i<=50000; i++);
/* and START
*(expansion) = 0x0;
*/
}
```

G.3 DSP Program lists for control of up to 6 2-level converters with phase shifted triangle carriers

Table G.2 and G.3 are the programs for DSP3 and DSP4 respectively, for control of multiconverters with phase shifted triangle carriers.

Table G.2: Program list for DSP3 to read data from one channel of A/D Converter and pass the data to DSP4 for feedback control.

```
*****************************************************
/* Program comdsp3.c, located in c:\hydra\multconv\source */
/* See comdsp4.c for description */
*****************************************************
#include "hydra.h"
#include "H_II_map.h" /* Definition of physical addresses */
#include "compt40.h"
#include "intpt40.h"
#define ACQ_START *expansion = 0x0
long *PhaseDiffDataOut;
long *ADconvDataOut;
volatile long Phase, Phase_new, Phase_old, VcoCount;
void c_int01(void)
/* interrupt from COMPORT 5 by DSP4 */
{
volatile long scratch;
ACQ_START;
 while(cp_in_level(5) != 0)
 {
 VcoCount = in_word(5);
 }
Phase_new = 0; Phase_old = Phase;
}
void c_int02(void) /* interrupts from BUSY_LOW */
{
int i;
if (cp_out_level(5) == 0)
{
out_word(*(expansion + 6),5);
}
}
main() {
  PhaseDiffDataOut = (long*)DSP3WRITEONLY;
  ADconvDataOut    = (long*)DSP3WRITEONLY+1;
  asm( "  push    ar0" ); /* Monitor doesn't do an IACK to the
right */
  asm( "  ldhi    4000h,ar0" ); /* address, so we need to do it
here */
  asm( "  iack    *ar0" );
  asm( "  pop     ar0" );

/* clear Semaphore 0 */
*Semaphore0 = 0x0;
if(cp_in_level(5) != 0) in_word(5);
setivec(IIOF0, c_int02);  /* set interrupt from BUSY_LOW */
asm( "  or    9h,iif" );        /* Setup and enable IIOF0 */
asm( "  andn  6h,iif" );
asm( "  and   0h,iie" );     /* disable all internal interrupts */
setivec(0x22, c_int01);  /* set interrupt vector */
set_iie(ICRDY5);  /* set to receive interrupts from COMPORT5
*/
GIE_ON();                          /* software enable interrupts
*/
while(1)
{
/* Main  Loop to wait for software interrupt from DSP4
and then hardware interrupt from ADC boards */
}
}
```

Table G.3: Program list for DSP4 for implementation of SPWM of 2-level multiconverters with phase shifted carriers.

```
/**************************************************
/* Program comdsp4.c, located in c:\hydra\multconv\source */
**************************************************
This program implements PWM control of the six 3-phase
2-level voltage source converters. The hardware periodic interrupt
to dsp4 is generated by the FPGA. The period of occurence of
the the hardware interrupt is programmed by loading PWM
Period register with a number. This number is calculated based
on the system clock, fundamental frequency, the number of
triangles, and the number of converters.
The Regualr sampling algorithm for multiconverter system
with phase shifted carriers has been implemented.
As from today, on May 22, 1996 the algorithm is working fine.
The algorithm can handle any even number of converters as per
FPGA design. It can handle one converter by setting the number
of converters equal to 2. For SVC operation, the control
algorithm is the same as for single module which is explained
below.

The DC voltage is regulated by a PI controller whch is in
theinterrupt routine. When dsp4 is interrupted, it writes the PWM
registers immediately, then it generates a software interrupt to
dsp3 by passing data through a comport. When dsp3 receives a
software interrupt from dsp4, it send a sample signal to the
ADC's, then reads the comport. Then the ADC's generate
hardware interrupt to dsp3, to signal that data conversion is
finished. Dsp3 then reads the data and pass them to dsp4. Dsp4
uses the data passed by dsp3 for feedback purposes. In order to
reduce delay, the writing of the PWM registers is done first for
every sampling instant.
*/

#include <math.h>
#define PI 3.1415926
#include "hydra.h"
#include "H_II_map.h" /* Definition of physical addresses */
#include "compt40.h"
#include "intpt40.h"
#define TableLen 4096 /* Length of sine table */
#define System_Clock 20000000
#define Mod_Freq 60 /* 60 Hz power system frequency */
#define Tri_Number 3 /* Number of triangles per 60 cycle */
#define Nd 6.0 /* Number of converter modules */

float m_index = 0.75; /* Modulation index */
float ModIndexf;
float Kp, Ki;
float Add_Mod_Kp, Add_Mod_Ki, Add_Mod_Ki_old;
int sinxi[4096], Tabx_out[13], Taby_out[12];
int Error_dc_voltage, Address_Corrector, pt_ref0, pt_ref1,
pt_ref2;
int f_triangle, f_sample, ModIndex, Add_Modifier;
int i, j, k, Nc, Nc1, Nc2, x1, x2, x3, x4;
int PWMCOUNT, SHIFT, counter;
int Vdc_ref, Vdc_limit, Vdc;
int C, Cn[3], Vm[3], Vm_old[3], kk[3];
volatile int *LevelAddress = (int *) 0x300010;
volatile long Phase, Temp, VcoCount, VcoCount_new;
unsigned int shift1; /* Start of Phase B */
unsigned int shift2; /* Start of Phase A */
unsigned int shift3; /* Start of Phase C */
void c_int01(void) /* interrupt Routine */
{
for(i = 0; i < 0xc; i++)
{
*(LevelAddress + i) = Taby_out[i];
}
for(i = 0; i < 0xd; i++)
{
*(LevelAddress + i) = Tabx_out[i];
}
/* *(LevelAddress + 0xc) = 0x0; Start PWM Counter */
/*
if(cp_out_level(1) == 0)
{
out_word(VcoCount,1); Generate software interrupt to dsp3 by
passing data through comport
}
*/
VcoCount = ((*VcoRefCounter) >> 16) - Address_Corrector;
/* PI controller
if(Temp > 13500)
*/
if(Temp > Vdc_limit)
Error_dc_voltage = Vdc_ref - Temp;
/*
Apply the controller only when adequate
dc voltage has been applied
*/
else Error_dc_voltage = Vdc_ref - Vdc;
/*
Bypass the controller when inadquate
dc voltage has been applied
*/
Add_Mod_Kp = (Kp*Error_dc_voltage);
Add_Mod_Ki = Add_Mod_Ki_old + (Ki*Error_dc_voltage);
if(abs(Add_Mod_Ki) < 800)
{
Add_Mod_Ki_old = Add_Mod_Ki;
VcoCount_new = VcoCount - (int)(Add_Mod_Kp +
Add_Mod_Ki);
}
else VcoCount_new = VcoCount - (int)(Add_Mod_Kp +
Add_Mod_Ki_old);
pt_ref0 = (VcoCount_new + shift3)%TableLen;
pt_ref1 = (VcoCount_new + shift1)%TableLen;
pt_ref2 = (VcoCount_new + shift2)%TableLen;
Vm[0] = sinxi[pt_ref2];
Vm[1] = sinxi[pt_ref1];
Vm[2] = sinxi[pt_ref0];
for(k = 0; k < 3; k++)
{
kk[k] = (kk[k] + 1)%Nc;
Taby_out[(4*k)] = 0xf0000;
Taby_out[(4*k) + 1] = 0xf0000;
for(i = 0; i < Nc2; i++)
{
if((Cn[i] > Vm[k]) && (Vm[k] >= Cn[i + 1]))
{
Tabx_out[(4*k)] = ((Nc + kk[k] - i)%Nc) << 16;
```

```
Tabx_out[(4*k) + 1] = ((kk[k] + i + 1)%Nc) << 16;
Tabx_out[(4*k) + 2] = (Cn[i] - Vm[k]) << 16;
Tabx_out[(4*k) + 3] = (Vm[k] - Cn[i + 1]) << 16;
if(Cn[i+1] > Vm_old[k])
/* Check for switching level cross over with positive slope */
{
Taby_out[(4*k)] = ((Nc + kk[k] - i - 1)%Nc) << 16;
}
if(Cn[i] < Vm_old[k])
/* Check for switching level cross over with negative slope */
{
Taby_out[(4*k) + 1] = ((kk[k] + i)%Nc) << 16;
}
}
}
Vm_old[k] = Vm[k];
}
while(1)
{
if(cp_in_level(1) != 0)
{
Temp = (in_word(1) >> 8) & (0x0ffff);
/* Get data from dsp3 through comport and eliminate the busy
signal
*/
break;
}
}
}

main() {
  asm( " push    ar0" ); /* Monitor doesn't do an IACK to the
right */
  asm( " ldhi    4000h,ar0" ); /* address, so we need to do it
here */
  asm( " iack    *ar0" );
  asm( " pop     ar0" );
shift1 = TableLen/3;
shift2 = (TableLen*2)/3;
shift3 = TableLen;
for(k = 0; k < 3; k++)
{
Taby_out[(4*k) + 2] = 0x0;
Taby_out[(4*k) + 3] = 0x0;
kk[k] = 0;
}
Tabx_out[12] = 0x0;
Nc = (int)(Nd);
Nc2 = Nc/2;
Nc1 = Nc2 + 1;
f_triangle = Mod_Freq*Tri_Number; /* Frequency of Triangular
carrier */
PWMCOUNT = System_Clock/(2*f_triangle);
counter = PWMCOUNT/Nc2;
SHIFT = PWMCOUNT/2;
C = 4*SHIFT/Nc;
for(i = 0; i < Nc1; i++)
{
Cn[i] = PWMCOUNT - (i*C); /* Compute the switching levels
*/
}
ModIndexf = SHIFT*m_index; /* Initialize the Modulation Index
*/
/* Calculate the modulating signal tables */
for (j=0; j<TableLen; j++)
        {
                sinxi[j] = SHIFT +
(int)(ModIndexf*sin(2*PI*j/TableLen));
        }
/*
for (j=0; j<TableLen; j++)
        {
                sinxi[j] = SHIFT +
(int)(ModIndexf*(sin(2*PI*j/TableLen) +
(0.35*sin(6*PI*j/TableLen))));
        }
*/
/*
x1 = TableLen/5;
x2 = TableLen/2;
x3 = x1 + x2;
x4 = -1;
for (j=0; j<TableLen; j++)
        {
          if(j <= x1) sinxi[j] = SHIFT + (int)(ModIndexf);
          else if((j > x2) && (j <= x3)) sinxi[j] = SHIFT -
(int)(ModIndexf);
          else sinxi[j] = SHIFT + (int)(2*(pow(x4, j)));
        }
*/
/* Vdc_ref = 14420; This number is equivalent to 100 volts read
by ADC voltage sensor board #4 */
Vdc_ref = 7234; /* This number is equivalent to 50 volts read by
ADC voltage sensor board #4 */
Vdc = Vdc_ref;
Temp = 0;
Vdc_limit = (floor)(Vdc_ref*0.850);
/* Address_Corrector = 800; */
Address_Corrector = 700;
/*
This number is added to the VcoRefCounter reading
to make the PWM voltage in phase with the power system
voltage
for a set point of 100 volts dc voltage
*/
Kp = 0.0025; /* Proportional control  Gain */
Ki = 0.0001; /* Integral control Gain  */
/*
Kp = 0.0025;
Ki = 0.00001;
*/
while(cp_in_level(1) !=0) in_word(1); /* Clear the comport */
*(PwmPeriodCounter) = (counter) << 16;
/* Set the multiconverter Sampling Period With Phase Shifted
Carriers */

*(LevelAddress + 0xc) = 0x0; /* Start PWM Counter */
*(PwmIntEnable) = 0x300; /* Enable hardware interrupts */
setivec(IIOF0,c_int01);    /* set interrupt vector */
asm( " or   9h,iif" );     /* setup to receive interrupt */
asm( " andn 6h,iif" );              /* define edge and clear */
GIE_ON();                           /* software enable interrupts
*/
while(1)
{
/* Main Loop: Wait for the hardware interrupt from FPGA */
}
```

G.4 DSP Program lists for control of 6-level converter

Table G.4 and G.5 are the programs for DSP3 and DSP4 respectively, for control of 6-level 3-phase converter (tested as Series VAR Compensator).

Table G.4: Program list for DSP3 to read data from 5 channels of A/D Converters and pass the data to DSP4 for feedback control. Only one channel of A/D converter is serviced per sample.

```
*************************************************
/* Program comdsp3.c, located in c:\hydra\multilev\source */
/* See comdsp4.c for description */
*************************************************
#include "hydra.h"
#include "H_II_map.h" /* Definition of physical addresses */
#include "compt40.h"
#include "intpt40.h"
#define ACQ_START *expansion = 0x0
long *PhaseDiffDataOut;
long *ADconvDataOut;
volatile long Phase, VcoCount;
int j, k, Vdcs[5];
void c_int01(void)
{
/* interrupts from COMPORT 5) */
ACQ_START;
 while(cp_in_level(5) != 0)
 {
 VcoCount = in_word(5);
 }
}
void c_int02(void)
{
/* interrupts from BUSY_LOW   */
Vdcs[k] = *(expansion + k + 1);
if (cp_out_level(5) == 0)
{
out_word(Vdcs[k],5); /* Pass data to dsp4 through comport #5 */
}
k = (k + 1)%5;
}
main()
{
PhaseDiffDataOut = (long*)DSP3WRITEONLY;
 ADconvDataOut   = (long*)DSP3WRITEONLY+1;
 asm( "  push    ar0" ); /* Monitor doesn't do an IACK to the
right */
 asm( "  ldhi    4000h,ar0" ); /* address, so we need to do it
here */
 asm( "  iack    *ar0" );
 asm( "  pop     ar0" );
/* clear Semaphore 0 */
*Semaphore0 = 0x0;
if(cp_in_level(5) != 0) in_word(5); /* Clear comport  #5 */
setivec(IIOF0, c_int02);        /* set interrupt from BUSY_LOW
*/
asm( "  or   9h,iif" );         /* Setup and enable IIOF0 */
asm( "  andn  6h,iif" );
asm( "  and   0h,iie" );          /* disable all internal interrupts
*/
setivec(0x22, c_int01);   /* set interrupt vector */
set_iie(ICRDY5);              /* set to receive interrupts from
COMPORT5 */
GIE_ON();   /* enable software interrupts */
k = 1;
while(1)
{
/* Main  Loop to wait for software interrupt from DSP4
and then hardware interrupt from ADC boards  */
}
}
```

Table G.5: Program list for DSP4 for implementation 6-level converter (tested as Series Static VAR Compensator).

```
*************************************************
/* Program comdsp4.c, located in c:\hydra\multilev\source */
*************************************************
```

This program implements Selected Harmonic Elimination (5th and 7th) Fundamental Switching control of the 3-phase 6-level voltage source converter. The hardware periodic interrupt to dsp4 is generated by the FPGA. The period of occurence of the hardware interrupt is determined by the period of bit 2, 3, 4 or 5 of the VCO Counter by loading PWM Period register. This way the 60 Hz signal is sampled 1024, 512, 256, or 128 times per cycle respectivly. The switching pattern has been designed in such a way that for each of the five slices, one writing is done for all the three phases. In this way, only 5 writes are required to be performed by the DSP4.

The DC voltages are regulated and equalized by PI controllers which are in the interrupt routine. When DSP4 is interrupted by FPGA, it writes the current switching pattern to the PWM registers immediately, then it generates a software interrupt to DSP3 by passing data through its comport #1. When DSP3 receives a software interrupt from DSP4, it send a sample signal to the ADC's, then reads its comport #5. Then the ADC's

```
generate hardware interrupt to DSP3, to signal
that data conversion is finished. DSP3 then reads the data and
pass them to DSP4. DSP4 uses the data passed by DSP3 for
feedback purposes. In order to reduce delay, the writing of the
PWM registers is done first for every sampling instant.
*/
/* #include <math.h> */
#include "hydra.h"
#include "H_II_map.h" /* Definition of physical addresses */
#include "compt40.h"
#include "intpt40.h"
#define TableLen 1024 /* Length of switching patterns */
#include "dt1new.h" /* Fisrt slice switching pattern */
#include "dt2new.h" /* Second slice switching pattern */
#include "dt3new.h" /* Third slice switching pattern */
#include "dt4new.h" /* Fourth slice switching pattern */
#include "dt5new.h" /* Fifth slice switching pattern */
float Kp, Ki, Kpp[5], Kii[5];
float Add_Mod_Kp, Add_Mod_Ki, Add_Mod_Ki_old;
float Add_Mod_Kpp[5], Add_Mod_Kii[5], Add_Mod_Kii_old[5];
int Error_dc_voltage, Error_dcs_voltage[5], lower_limit;
int Add_Modifier[5], Address_Corrector;
int i, k, j, Vdc, Vdc1, Vdcs[5], Vdc_ref, Vdc_refs[5];
int switches, switch_on, kn;
unsigned int pt_ref0[5];
volatile long Temp, VcoCount;
unsigned int shift0; /* Start of Phase A */
void c_int01(void) /* interrupt Routine */
{
*(PwmRegister + 0) = tablex1[pt_ref0[0]];
*(PwmRegister + 1) = tablex2[pt_ref0[1]];
*(PwmRegister + 2) = tablex3[pt_ref0[2]];
*(PwmRegister + 3) = tablex4[pt_ref0[3]];
*(PwmRegister + 4) = tablex5[pt_ref0[4]];
/*
if(cp_out_level(1) == 0)
{
out_word(VcoCount,1);
}
*/
/* Generate software interrupt to dsp3 by passing data through
comport */
VcoCount = ((*VcoRefCounter) >> 18) - Address_Corrector;
/* PI controller is done to one capacitor voltage per sample */
/* Perform the control only if the voltage has been applied to the
sensors */
if(Temp > lower_limit)
{
/* Vdcs[k] = Vdcs[k]*0.5 + Temp*0.5; */
Vdcs[k] = Temp;
/* Error_dc_voltage = Vdc_ref - Vdc1; */
/* Error_dcs_voltage[k] = Vdc_refs[k] - Vdcs[k]; */
/* Lagging VAR Compensation */
Error_dc_voltage = Vdc1 - Vdc_ref;
Error_dcs_voltage[k] = Vdcs[k] - Vdc_refs[k];
/* Leading VAR Compensation */
Add_Mod_Kp = (Kp*Error_dc_voltage);
Add_Mod_Kpp[k] = (Kpp[k]*Error_dcs_voltage[k]);
Add_Mod_Ki = Add_Mod_Ki_old + (Ki*Error_dc_voltage);
Add_Mod_Kii[k] = Add_Mod_Kii_old[k] +
(Kii[k]*Error_dcs_voltage[k]);
/* if(abs(Add_Mod_Ki ) < 50) To avoid troubles, don't change
this limit */
if(abs(Add_Mod_Ki ) < 150)
{
Add_Mod_Ki_old = Add_Mod_Ki;
Add_Modifier[k] = (int)(Add_Mod_Kp + Add_Mod_Ki);
}
else Add_Modifier[k] = (int)(Add_Mod_Kp +
Add_Mod_Ki_old);
if(abs(Add_Mod_Kii[k]) < 5) /* To avoid troubles, don't change
this limit */
{
Add_Mod_Kii_old[k] = Add_Mod_Kii[k];
Add_Modifier[k] = Add_Modifier[k] + (int)(Add_Mod_Kpp[k]
+ Add_Mod_Kii[k]);
}
else Add_Modifier[k] = Add_Modifier[k] +
(int)(Add_Mod_Kpp[k] + Add_Mod_Kii_old[k]);
}
for(i=0; i<5; i++)
        {
        pt_ref0[i] = ((VcoCount - Add_Modifier[i]) +
shift0)%TableLen;
        Vdc = Vdc + Vdcs[i];
        }
Vdc1 = Vdc;
Vdc = 0;
k = (k + 1)%5;
/*
kn = (kn + 1)%switches;
if(kn >= switch_on) *(PwmIntEnable) = 0x200;
else *(PwmIntEnable) = 0x300;
This implements periodic turn on and turn off of the converter.
*/
/*
while(1)
{
if(cp_in_level(1) != 0)
{
Temp = (in_word(1) >> 8) & (0x0ffff);
break;
}
}
*/
/* Get data from dsp3 through comport #1 and eliminate the busy
signal */
}

main()
{
 asm( "  push    ar0" ); /* Monitor doesn't do an IACK to the
right */
 asm( "  ldhi    4000h,ar0" ); /* address, so we need to do it
here */
 asm( "  iack    *ar0" );
 asm( "  pop     ar0" );
setivec(IIOF0,c_int01);    /* set interrupt vector */
asm( " or   9h,iif" );     /* setup to receive interrupt */
asm( " andn 6h,iif" );              /* define edge and clear */
GIE_ON();                           /* software enable interrupts
*/
/* shift0 = TableLen/2; */
shift0 = TableLen;
Address_Corrector = 100;
/*
This number is added to the VcoRefCounter reading
to make the output voltage to be in phase with the power system
```

```
voltage */
/* Vdc_ref = 44413;; This number is equivalent to 150 volts */
/* These numbers are equivalent to 30 volts
read by ADC voltage sensor boards as indicated.
The ADC's used are, from top to bottom:
ADC #6, ADC #3, ADC #4, ADC #5 and ADC #1 respectively.
*/
Vdc_refs[0] = 9533;
Vdc_refs[1] = 8891;
Vdc_refs[2] = 8501;
Vdc_refs[3] = 8721;
Vdc_refs[4] = 8768;
k = 0;
Temp = Vdc_refs[0];
lower_limit = (int)(0.7*Vdc_refs[0]);
Vdcl = Vdc_ref;
Vdc = 0;
Kp = 0.005;
/* Proportinal control  Gain */
Ki = 0.0001;
/* Integral control Gain  */
/*
Kp = 0.0025;
Ki = 0.00001;
*/
for(i=0; i<5; i++)
{
/*
Kpp[i] = 0.0001;
Kii[i] = 0.00001;
*/
Kpp[i] = 0.0004;
Kii[i] = 0.00002;
Add_Mod_Kpp[i] = 0;
Add_Mod_Kii[i] = 0;
Add_Modifier[i] = 0;
}
Add_Mod_Ki = 0;
switches = 5*30720;
switch_on = 4.5*30720;
kn = 0;
while(cp_in_level(1) !=0) in_word(1);
/* Clear comport  #1 */
/* *(PwmPeriodCounter) = 0x10000; */
/* Set the sampling Period to 1024 samples per 60Hz cycle */
*(PwmPeriodCounter) = 0x20000;
/* Set the sampling Period to 512 samples per 60Hz cycle */
/* *(PwmPeriodCounter) = 0x40000; */
/* Set the sampling Period to 256 samples per 60Hz cycle */
/* *(PwmPeriodCounter) = 0x80000; */
/* Set the sampling Period to 128 samples per 60Hz cycle */
*(PwmIntEnable) = 0x300;  /* enable hardware interrupts */
while(1)
{
/* Main Loop: Wait for the hardware interrupt from FPGA */
}
}
```

F.5 DSP Program lists for control of two 4-level converters as 6-phase system

Table G.6 and G.7 are the programs for DSP3 and DSP4 respectively, for control of 2 4-level 3-phase converters in 6-phase mode (tested as Shunt VAR Compensator).

Table G.6: Program list for DSP3 to read data from 3 channels of A/D Converters and pass the data to DSP4 for feedback control. Only one channel of A/D converter is serviced per sample.

```
**************************************************
/* Program comdsp3.c, located in c:\hydra\fmultlev\source */
/* See comdsp4.c for description */
**************************************************
#include "hydra.h"
#include "H_II_map.h"
#include "compt40.h"
#include "intpt40.h"
#define ACQ_START *expansion = 0x0
long *PhaseDiffDataOut;
long *ADconvDataOut;
volatile long Phase, VcoCount;
int j, k, Vdcs[3];
void c_int01(void)
{
/* volatile long Phase_new, Phase_old; */
/* interrupts from COMPORT 5) */
ACQ_START;
 while(cp_in_level(5) != 0)
 {
 VcoCount = in_word(5);
 }
}
void c_int02(void)
{
/* interrupts from BUSY_LOW  */
Vdcs[k] = *(expansion + k + 1);
if (cp_out_level(5) == 0)
{
out_word(Vdcs[k],5); /* Pass data to dsp4 through comport #5 */
}
k = (k + 1)%3;
```

```
}

main()
{
  PhaseDiffDataOut = (long*)DSP3WRITEONLY;
  ADconvDataOut    = (long*)DSP3WRITEONLY+1;
  asm( "  push    ar0" ); /* Monitor doesn't do an IACK to the
right */
  asm( "  ldhi    4000h,ar0" ); /* address, so we need to do it
here */
  asm( "  iack    *ar0" );
  asm( "  pop     ar0" );
/* clear Semaphore 0 */
*Semaphore0 = 0x0;
if(cp_in_level(5) != 0) in_word(5); /* Clear comport  #5 */
setivec(IIOF0, c_int02);        /* set interrupt from BUSY_LOW
*/
asm( "  or    9h,iif" );        /* Setup and enable IIOF0 */
asm( "  andn  6h,iif" );
asm( "  and   0h,iie" );          /* disable all internal interrupts
*/
setivec(0x22, c_int01);   /* set interrupt vector */
set_iie(ICRDY5);              /* set to receive interrupts from
COMPORT5 */
GIE_ON();                         /* enable software interrupts
*/
k = 1;
while(1)
{
/* Main  Loop to wait for software interrupt from DSP4
and then hardware interrupt from ADC boards  */
}
}
```

Table G.7: Program list for DSP4 for implementation of two 4-level 3-phase converters in 6-phase mode (tested as Shunt VAR Compensator).

```
*************************************************
/* Program comdsp4.c, located in c:\hydra\fmultlev\source */
*************************************************
```

This program implements Selected Harmonic Elimination (5th) Fundamental Switching control of two 3-phase 4-level voltage source converters as six phase system. The hardware periodic interrupt to DSP4 is generated by the FPGA. The period of occurence of the hardware interrupt is determined by the period of bit 2, 3, 4 or 5 of the VCO Counter by loading PWM Period register. This way the 60 Hz signal is sampled 1024, 512, 256, or 128 times per cycle respectivly. The switching pattern has been designed in such a way that for each of the three slices for both converters, one writing is done for all the three phases. In this way, only 3 writes are required to be performed by the DSP4.

The DC voltages are regulated and equalized by PI controllers which are in the interrupt routine. When DSP4 is interrupted by FPGA, it writes the current switching pattern to the PWM registers immediately, then it generates a software interrupt to DSP3 by passing data through its comport #1. When DSP3 receives a software interrupt from DSP4, it send a sample signal to the ADC's, then reads its comport #5. Then the ADC's generate hardware interrupt to DSP3, to signal that data conversion is finished. DSP3 then reads the data and pass them to DSP4. DSP4 uses the data passed by DSP3 for feedback purposes. In order to reduce delay, the writing of the PWM registers is done first for every sampling instant.

```
*/
/* #include <math.h> */
#include "hydra.h"
#include "H_II_map.h"
#include "compt40.h"
#include "intpt40.h"
#define TableLen 1024
/*
#include "dtm1new.h"
#include "dtm2new.h"
#include "dtm3new.h"
*/
#include "six1.h"
#include "six2.h"
#include "six3.h"
float Kp, Ki, Kpp[3], Kii[3];
float Add_Mod_Kp, Add_Mod_Ki, Add_Mod_Ki_old;
float Add_Mod_Kpp[3], Add_Mod_Kii[3], Add_Mod_Kii_old[3];
int Error_dc_voltage, Error_dcs_voltage[3], lower_limit;
int Add_Modifier[3], Address_Corrector;
int i, k, j, Vdc, Vdc1, Vdcs[3], Vdc_ref, Vdc_refs[3];
unsigned int pt_ref0[3];
volatile long Temp, VcoCount;
unsigned int shift0; /* Start of Phase A */
void c_int01(void) /* interrupt Routine */
{
*(PwmRegister + 0) = tablex1[pt_ref0[0]];
*(PwmRegister + 1) = tablex2[pt_ref0[1]];
*(PwmRegister + 2) = tablex3[pt_ref0[2]];
if(cp_out_level(1) == 0)
{
out_word(VcoCount,1);
}
/* Generate software interrupt to DSP3 by passing data through
comport */
VcoCount = ((*VcoRefCounter) >> 18) - Address_Corrector;
/* PI controller is done to one capacitor voltage per sample */
/* Perform the control only if the voltage has been applied to the
sensors */
if(Temp > lower_limit)
{
/* Vdcs[k] = Vdcs[k]*0.5 + Temp*0.5; */
Vdcs[k] = Temp;
Error_dc_voltage = Vdc_ref - Vdc1;
/* Error_dcs_voltage[k] = Vdc_refs[k] - Vdcs[k]; */
/* Lagging VAR Compensation */
Error_dcs_voltage[k] = Vdcs[k] - Vdc_refs[k];
/* Leading VAR Compensation */
Add_Mod_Kp = (Kp*Error_dc_voltage);
Add_Mod_Kpp[k] = (Kpp[k]*Error_dcs_voltage[k]);
Add_Mod_Ki = Add_Mod_Ki_old + (Ki*Error_dc_voltage);
Add_Mod_Kii[k]  =  Add_Mod_Kii_old[k]  +
```

```
(Kii[k]*Error_dcs_voltage[k]);
if(abs(Add_Mod_Ki ) < 150) /* To avoid troubles, don't change
this limit */
{
Add_Mod_Ki_old = Add_Mod_Ki;
Add_Modifier[k] = (int)(Add_Mod_Kp + Add_Mod_Ki);
}
else Add_Modifier[k] = (int)(Add_Mod_Kp +
Add_Mod_Ki_old);
if(abs(Add_Mod_Kii[k]) < 5) /* To avoid troubles, don't change
this limit */
{
Add_Mod_Kii_old[k] = Add_Mod_Kii[k];
Add_Modifier[k] = Add_Modifier[k] + (int)(Add_Mod_Kpp[k]
+ Add_Mod_Kii[k]);
}
else Add_Modifier[k] = Add_Modifier[k] +
(int)(Add_Mod_Kpp[k] + Add_Mod_Kii_old[k]);
}
for(i=0; i<3; i++)
        {
        pt_ref0[i] = ((VcoCount - Add_Modifier[i]) +
shift0)%TableLen;
        Vdc = Vdc + Vdcs[i];
        }
Vdc1 = Vdc;
Vdc = 0;
k = (k + 1)%3;
while(1)
{
if(cp_in_level(1) != 0)
{
Temp = (in_word(1) >> 8) & (0x0ffff);
break;
}
}
/* Get data from DSP3 through comport #1 and eliminate the
busy signal */
}

main()
{
 asm( "  push    ar0" ); /* Monitor doesn't do an IACK to the
right */
 asm( "  ldhi    4000h,ar0" ); /* address, so we need to do it
here */
 asm( "  iack    *ar0" );
 asm( "  pop     ar0" );
setivec(IIOF0,c_int01);   /* set interrupt vector */
asm( " or   9h,iif" );    /* setup to receive interrupt */
asm( " andn 6h,iif" );              /* define edge and clear */
GIE_ON();                           /* software enable interrupts
*/
shift0 = TableLen;
Vdc_ref = 34521;
/* This is equivalent to a total of 120 volts */
Vdc_refs[0] = 11503;
Vdc_refs[1] = 11475;
Vdc_refs[2] = 11547;
/* These numbers are equivalent to 40 volts
read by ADC voltage sensor boards as indicated.
The ADC's used are, from top to bottom:
ADC #4, ADC #5 and ADC #1 respectively.
*/
k = 0;
Temp = Vdc_refs[0];
lower_limit = (int)(0.7*Vdc_refs[0]);
Vdc1 = Vdc_ref;
Vdc = 0;
Address_Corrector = 50;
/*
This number is added to the VcoRefCounter reading
to make the PWM voltage in phase with the power system
voltage
for a set point of 100 volts dc voltage
*/
Kp = 0.00025;
Ki = 0.00001;
/* Proportinal and Integral control Gains for the major feedback
loop */
/*
Kp = 0.00025;
Ki = 0.00001;
*/
for(i=0; i<3; i++)
{
Kpp[i] = 0.00001;
Kii[i] = 0.000001;
/*
Kpp[i] = 0.00001;
Kii[i] = 0.000001;
*/
/* Proportinal and Integral control Gains for the minor feedback
loops */
Add_Mod_Kpp[i] = 0;
Add_Mod_Kii[i] = 0;
Add_Modifier[i] = 0;
}
Add_Mod_Ki = 0;
while(cp_in_level(1) !=0) in_word(1); /* Clear comport #1 */
/* *(PwmPeriodCounter) = 0x10000; */
/* Set the sampling Period to 1024 samples per 60Hz cycle */
*(PwmPeriodCounter) = 0x20000;
/* Set the sampling Period to 512 samples per 60Hz cycle */
/* *(PwmPeriodCounter) = 0x40000; */
/* Set the sampling Period to 256 samples per 60Hz cycle */
/* *(PwmPeriodCounter) = 0x80000; */
/* Set the sampling Period to 128 samples per 60Hz cycle */
*(PwmIntEnable) = 0x300;  /* enable hardware interrupts */
while(1)
{
/* Main Loop: Wait for the hardware interrupt from FPGA */
}
}
```

APPENDIX H

PARAMETERS USED FOR SIMULATIONS

H.1 Simulation parameters based on each converter in the simulation studies of 6-phase and 12-phase STATCOMS

V_{base} = 26kV, S_{base} = 35MVA.

Outer loop proportional gain: Kp = 0.000001275 V^{-1}.

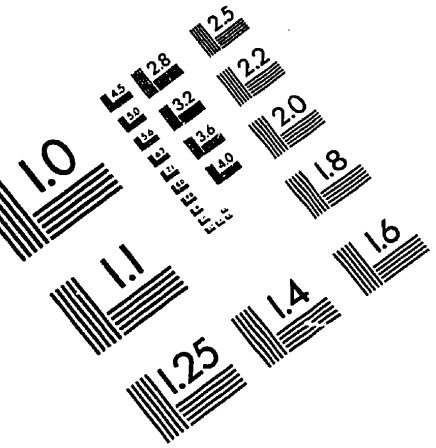
Outer loop integral gain: Ki = 0.0005 $V^{-1}s^{-1}$.

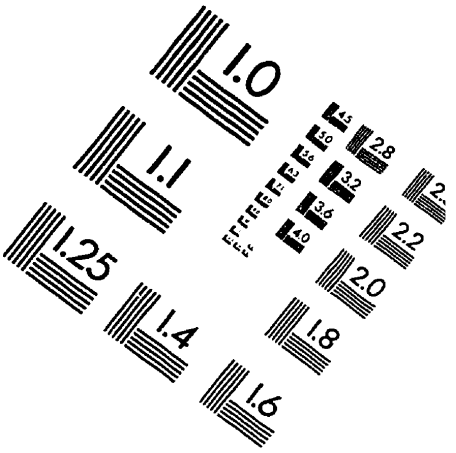
Inner loops proportional gains: Kpp = 0.0000005275 V^{-1}. Inner loops integral gains: Kii = 0.008 $V^{-1}s^{-1}$.

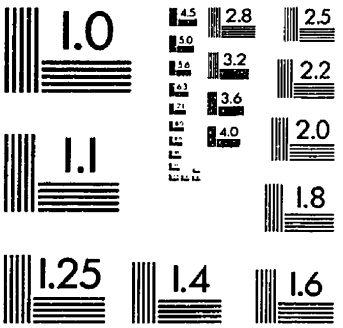
Dc link capacitors: $X_{c1} = X_{c2} = X_{c3} = X_{c4}$ = 0.23p.u.

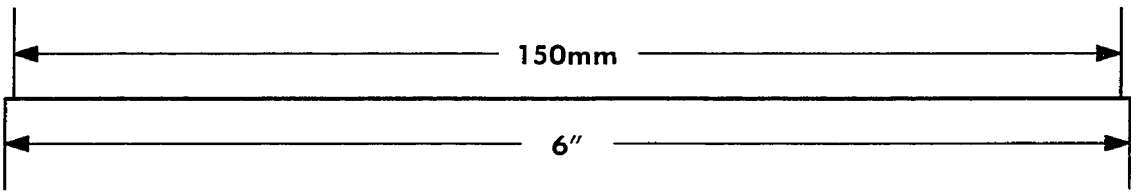
Ac side filter inductances: X_f = 0.1p.u., R_f = 0.02p.u.

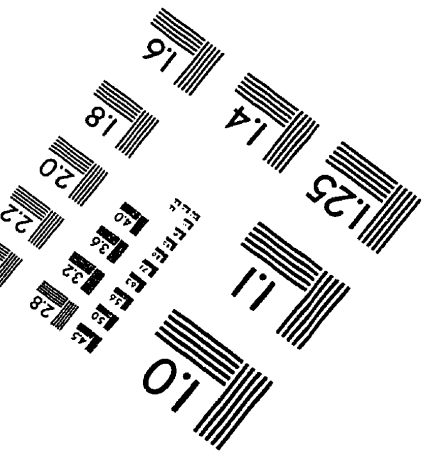
IMAGE EVALUATION
TEST TARGET (QA-3)











APPLIED IMAGE, Inc
1653 East Main Street
Rochester, NY 14609 USA
Phone: 716/482-0300
Fax: 716/288-5989

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