CONSTRUCTION AND TEST OF A DELTA MODULATED BUCK TYPE 3 PHASE CONVERTER

by

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ABSTRACT

A Delta Modulated, Buck Type, Three Phase PWM Converter was constructed and tested. The converter is of the current source type and can be used in conjunction with current source inverters.

The d.c. current is regulated by proportional feedback control loop. By delta modulation of the voltages across the a.c. terminals of the converter, the a.c. source currents are "indirectly" controlled so that the fundamental components remain in a predefined phase with respect to the source voltages.

Test results have shown that the converter draws near sinusoidal a.c. currents at unity power factor, with leading power factor a possibility.

RESUME

Un convertisseur triphasé produisant une tension continue à l'aide d'un montage de type abaisseur de tension, avec une commande en modulation de largeur d'impulsions, a été construit et testé. Le convertisseur fonctionne en source de courant et peut être utilisé avec un onduleur du même type.

Le courant continu est régularisé par une boucle de rétroaction proportionnelle. Le déphasage des courants alternatifs est indirectement commandé par une modulation de type Delta des tensions d'entrée du convertisseur

Les résultats démontrent que le convertisseur absorbe un courant alternatif presque sinusoïdal, avec un facteur de puissance unitaire. Un facteur de puissance capacitif est possible.

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NOMENCLATURE

BD	Base drive unit
BDL	Base drive logic
CVM	Capacitor voltage measurement
DC-CMC	DC current measurement circuit
D_p	Inter-phase diode
δ	Power angle
δt_1	Voltage raise time period
δt_2	Voltage lower time period
e_R, e_S, e_T	Three phase a.c. source voltages
ϵ	Error signal
GTO	Gate turn off thyristor
h	Voltage bandwidth (voltage window)
i_1	Buck type converter a.c. source current
i_{11}	Boost type converter d.c. link current
i_2	Buck type converter input current
i_{22}	Boost type converter load current
I_1	R.M.S. a.c. source current
i_4	Buck type converter d.c. link current
I_{c1}, I_{c2}	Opto-coupler collector currents
I_{F1}, I_{F2}	Opto-coupler diode currents
I_p	Peak a.c. source current
I_{REF}	DC link control reference current
K_p	DC link current controller gain
L_1	AC source inductance
L_2	DC link inductance
m1	T_1 transistor group modulate signal

m2	T_2 transistor group modulate signal
MBDL	Modified base drive logic
MVC	Modified voltage comparison
PWM	Pulse width modulation
Q1	Logic signal to T_1 base drive
Q2	Logic signal to T_2 base drive
R_1	AC source resistance
R_2	DC link resistance
RMS	Root-mean square
SI	Static Induction
v,V	Phase reference voltage
v_1, V_1	A.C. source voltage
v_c, V_c	Capacitor voltage
VC	Voltage comparison
V_l	Voltage lower signal
V^l	Lower reference bound
V_p	Peak a.c. source voltage
V_r	Voltage raise signal
V_R, V_S, V_T	Three phase voltage templates
V_{Ri}, V_{Si}, V_{Ti}	Three phase current templates
V^u	Upper reference bound
VTD	Voltage template derivation circuit
V_t	Instantaneous d.c. voltage
T_1	Positive half cycle transistor group
T_2	Negative half cycle transistor group
	Angular velocity

CHAPTER I

INTRODUCTION

1.1 OVERVIEW OF CONVERTER TECHNOLOGY

In the past decades, there has been extensive research activities done in the area of motor drive applications of power electronics. Among them, the researchers paid attention to topics such as (1) Harmonic elimination by application of improved PWM techniques and high speed switches, (2) The application of new switching devices such as GTOs, Power bipolar transistors, MOSFETs, Static Induction (SI) transistors and thyristors, etc., (3) The development of high performance control scheme such as vector control, and (4) the application of digital techniques especially microprocessors and microcontrollers to the control of the drives. Such developments have greatly improved the performance of the motor drives, d.c.-d.c. choppers, d.c.-a.c. inverters and the control schemes.

In recent years a new converter technology referred to as resonant power-processing technique has emerged. The core advantages of this new technique are zero switching losses and Source/Load isolation. The switching frequencies are well above those used in PWM techniques. In this new technique one can see the evolution of many generations of new ideas: Parallel resonant inverters/converters, Series resonant inverters/converters [1-14].

By comparison, there is still more research activities to be done on the utility a.c. to consumer d.c. interface. To date, the line commutated thyristor converter has remained the standard means of controlled a.c.-d.c. conversion especially for high power applications. With falling prices of fast switching high power transistors, MOSFETs, SI transistors/thyristors and GTO's, there is bright future for PWM converters as replacements to the classical line commutated thyristor converters. This revolution becomes more pronounced when considering the high tariffs charged by utility companies against excessive VAR consumption and the foreseeable threat of stricter harmonic standards which sooner or later will be imposed to the consumers.

At the present time there exist several AC-DC converter topologies but all of them can be grouped into two major categories: Current Source and Voltage Source converters as shown in Fig.1.1 and 1.2 respectively [15].

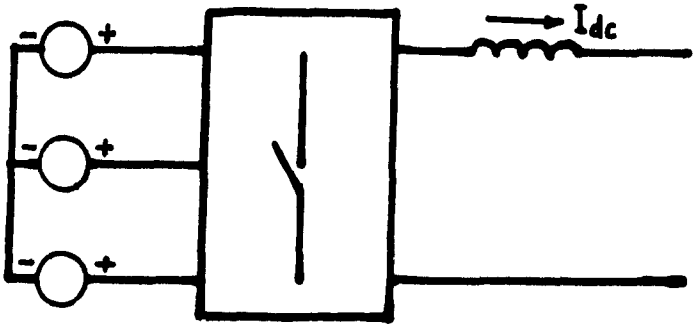


Fig.1.1 Current Source Converter.

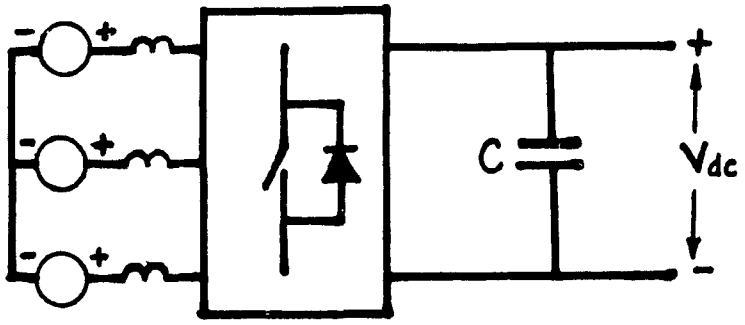


Fig.1.2 Voltage Source Converter.

Current source converter has AC voltage source input and DC current source output. Voltage source converter has AC current source input and DC voltage source output.

Since the introduction of PWM concept in motor drives applications and power electronics, a number of techniques have been developed [15,16-28]. The choice of PWM technique depends on topology, application and performance requirement(s) of the converter.

To this day there are several articles for prospective high performance PWM converters; but there is a tendency of the majority of researchers to concentrate in developing voltage source type of PWM converters [15,29-34]. The presence of conventional line commutated current source thyristor converters might have resulted in very few researchers devoting their time to developing current source

type of PWM converters [21,35-39]. This situation may lead to the line commutated thyristor converters remaining superior even in low power applications for some years to come whenever a highly inductive d.c. circuit exists. On contrary, most of the high performance inverters already developed are of the current source type which are widely applied in variable speed drive systems. This trend indicates that most of the researchers forget the issue of harmonic pollution to the utility supply and the punitive tariffs charged for excessively reactive power consumption caused by line commutated current source thyristor converters [33].

1.2 PROPOSED SCHEME

The objectives of this thesis are to construct a laboratory size of the proposed converter and to test it to verify the following features:

(1) Sinusoidal AC phase currents at the input and smooth DC current at the output.

(2) Unity power factor operation with the possibility of power factor regulation.

(3) Regulated DC current.

Fig.1.3 shows the single phase bridge of the proposed converter configuration. The single phase bridges of the converter are fed through three, single phase isolating transformers.

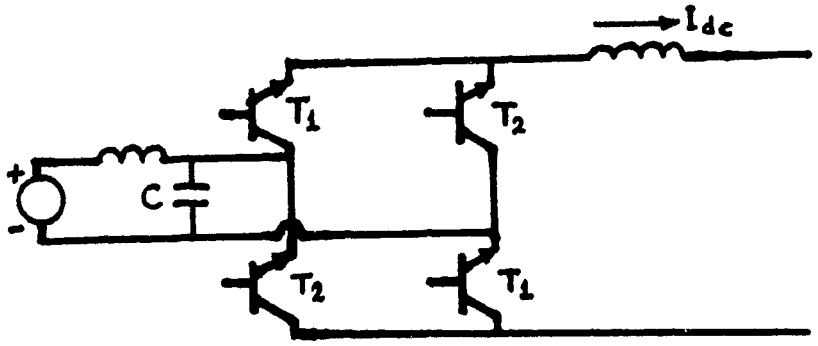


Fig.1.3 Single phase bridge of the proposed converter.

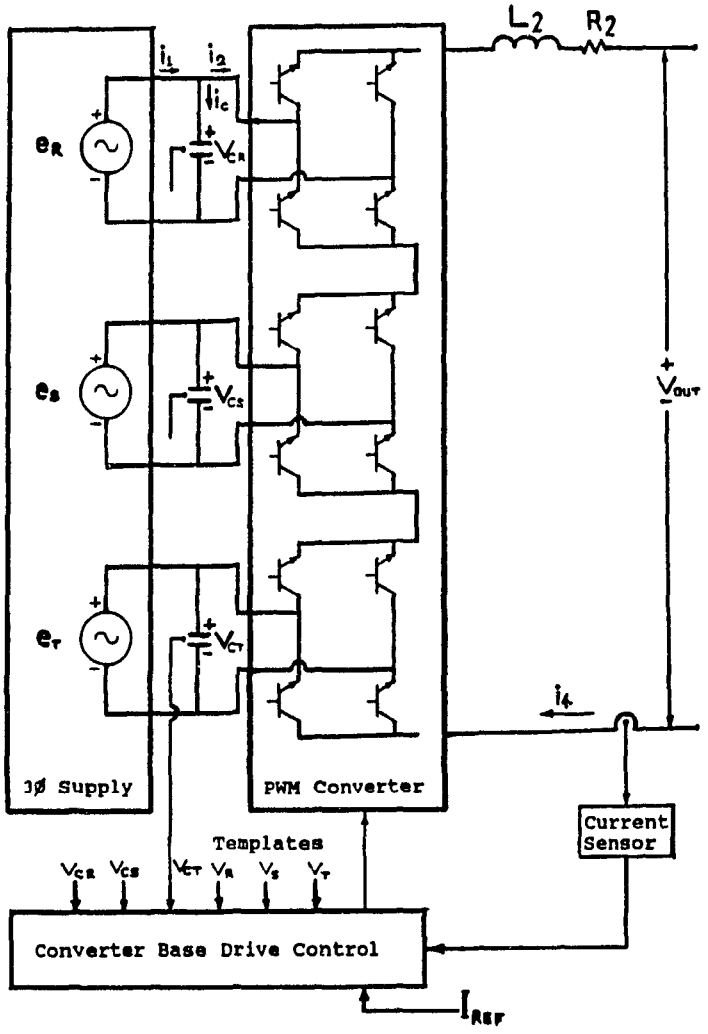


Fig.1.4 Proposed converter configuration.

The three, single phase bridges are then connected in series. Fig.1.4 shows, in compact form, the configuration of the proposed three phase PWM converter.

The DC current is regulated by reference current signal through a proportional feedback current control. The capacitor voltage is measured and controlled to follow the template within a pre-determined tolerance. This converter have been developed by translating the circuit of the controlled current boost type PWM converter [15,30,33] which is shown in Fig.1.5.

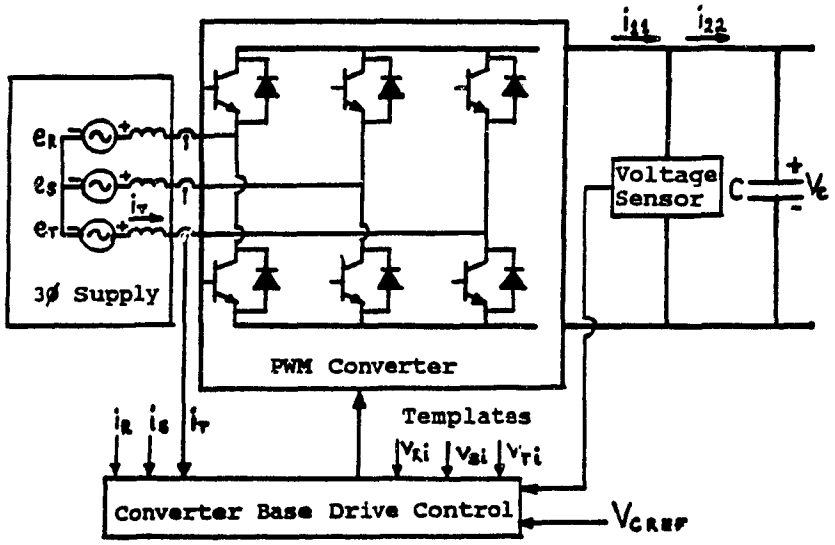


Fig.1.5 Controlled Current Boost type PWM Converter.

In the controlled current PWM converter which is of the voltage source type, the d.c. voltage is common to all three phases. The "dual" translation for this, is to make the d.c. current common to all three phases. The dual concept

unifies the Buck type (Current Source) and the Boost type (Voltage Source) converters. This buck type converter have been developed in consideration of the need of high performance current source converter which may gradually replace the conventional line commutated thyristor converter. The duality is finally accomplished by replacing "Current Hysteresis Control" with "Voltage Hysteresis Control" which is referred as "Delta Modulation Control" [15]. The power input is made to track the demand of the d.c. link by feedback control in which the converter adjusts the power level to ensure that the d.c. current is regulated.

This thesis presents the preliminary work on this converter topology. Test results have shown that the converter draws nearly sinusoidal a.c. currents and exhibits unity power factor with possibility of leading power factor.

Since the control is based on voltage hysteresis, this converter is referred as "Delta Modulated Converter" [15,16]. Delta Modulation technique is mainly applied to Static Power Inverters [24,28,40,41].

Several PWM converter topologies consists of a.c. capacitors. Since one of the purposes of the PWM technique is to suppress lower order harmonics, these a.c. capacitors normally serve as higher order harmonic filters so as to achieve nearly sinusoidal a.c. source currents [35,36,38,42].

In current source PWM converters, the a.c. capacitors have an additional function of suppressing the switching transients caused by a.c. source inductance [35,36,38,43].

In addition to the above listed functions, in this thesis the a.c. capacitor across each phase is used to measure the voltage which is made to track the template. The capacitor voltage is compared with two sinusoidal reference bounds and the error is used to generate switching signals. In this way, the control scheme becomes simple and could be implemented by analogue circuitry.

An immediate comparative advantage of this topology is that the converter is self starting as opposed to its dual topology [29-33].

1.3 SUMMARY OF WORK UNDERTAKEN

The objectives of this thesis are to construct and to test the proposed PWM converter capable of drawing 3-phase sinusoidal a.c. currents at unity power factor with d.c. current regulation.

The converter built was limited to laboratory size because the topology used is new and detailed investigation of its versatility has to be done before an industrial size converter can be considered. Test results presented in this thesis were obtained under steady state conditions.

1.4 ORGANIZATION OF THE THESIS

Chapter II presents the principles of delta modulation control and its circuit implementation. The outer DC current regulation feedback loop is described and the requirements for each stage in the loop are given. The inner delta feedback loop consisting of capacitor voltage measurement (CVM) and voltage comparison (VC) is described. The circuit implementation of each stage in the DC current (outer feedback loop) and capacitor voltage (inner feedback loop) are covered. The stages are:

(i) Voltage Template Derivation

(ii) DC Current Feedback

(iii) Voltage Reference Generator (VRG)

(iv) Capacitor Voltage Measurement (CVM)

(v) Voltage Comparison (VC)/(MVC)

(vi) Base Drive Logic (BDL)/(MBDL)

Chapter III describes the PWM switch modules consisting of the bipolar transistors, the snubber protection and the base drive (BD) units.

Chapter IV gives a brief description of operating modes of the converter. In addition the range of parameter values used during the tests are given.

Chapter V presents the test results of balanced three phase steady state operation. The test results are

illustrated by photographs taken from the oscillograms. A resistor was used as a load on the DC link.

Chapter VI gives the conclusions of this thesis and suggestions for further work.

CHAPTER II

DELTA MODULATION CONTROL PRINCIPLES

This chapter presents the principles of delta modulation (voltage hysteresis) control and the circuits used for its implementation.

With this topology, the necessary condition for satisfactory operation is to make sure that the d.c. current path is not blocked. To ensure this, two alternative strategies are presented and their merits are discussed in detail. The first strategy used is that while T_1 transistor group modulate, T_2 transistor group stays on all the time and vice-versa (Fig.3.1). Moreover the on state of T_1 transistor group and T_2 transistor group overlap for the period of zero crossing of the voltage hysteresis window. The second strategy used is to switch the two transistor groups ON and OFF alternatively according to logic command signals V_r and V_l. At the same time a short overlap period is given between on state of the incoming transistor group and off state of the outgoing transistor group in a single phase bridge.

2.1 PRINCIPLE OF OPERATION

The a.c. capacitors across each phase of the power circuit serve two purposes: First, they act as low pass filters. The second function is the core of the modulation principle of this converter. That is modulation takes place by charging and discharging the capacitor. In this way the

capacitor voltage is confined within pre-determined limits above and below the sinusoidal waveform template (see Fig.2.2).

The principle of operation can be explained with the help of Fig.2.1 and 2.2. For the purpose of explanation, phase "R" is used as a reference.

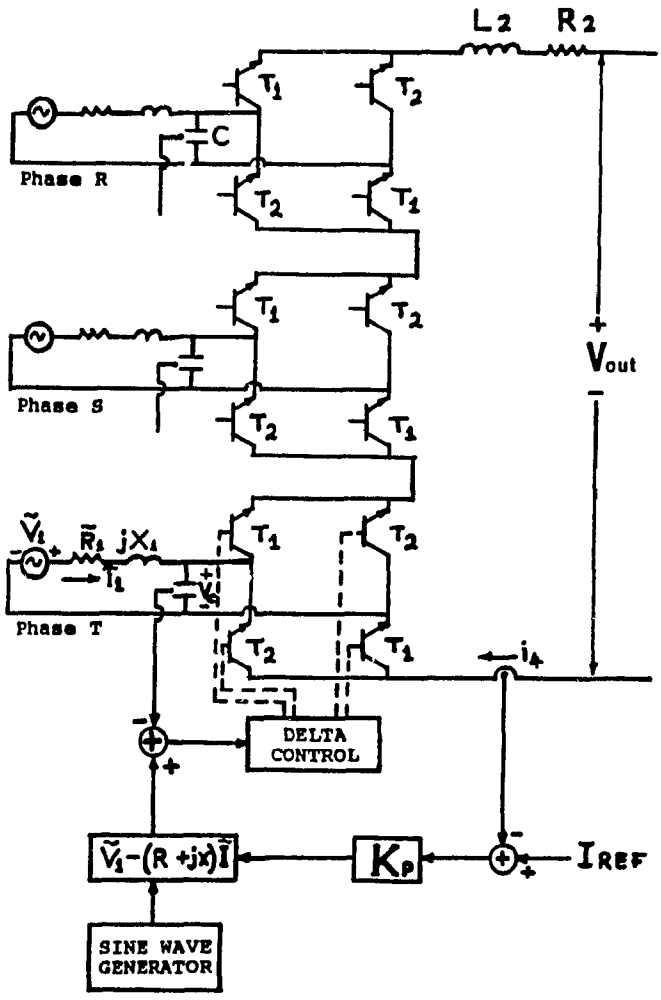


Fig.2.1 Delta Modulation Control Circuit.

First the reference signal V is derived using the three phase utility supply and d.c. current feedback. The voltage window "h" is introduced to prescribe upper and lower bounds, V^u and V^l. The actual phase capacitor voltage v_c is measured and made to track the reference signal V by ON-OFF switching of the transistor groups T_1 and T_2 in the H-bridge. Whenever the capacitor voltage tends to exceed the upper bound, the Base Drive Control Logic will produce a switching action to reduce it. An opposite switching action will occur when the capacitor voltage tends to go below the lower bound.

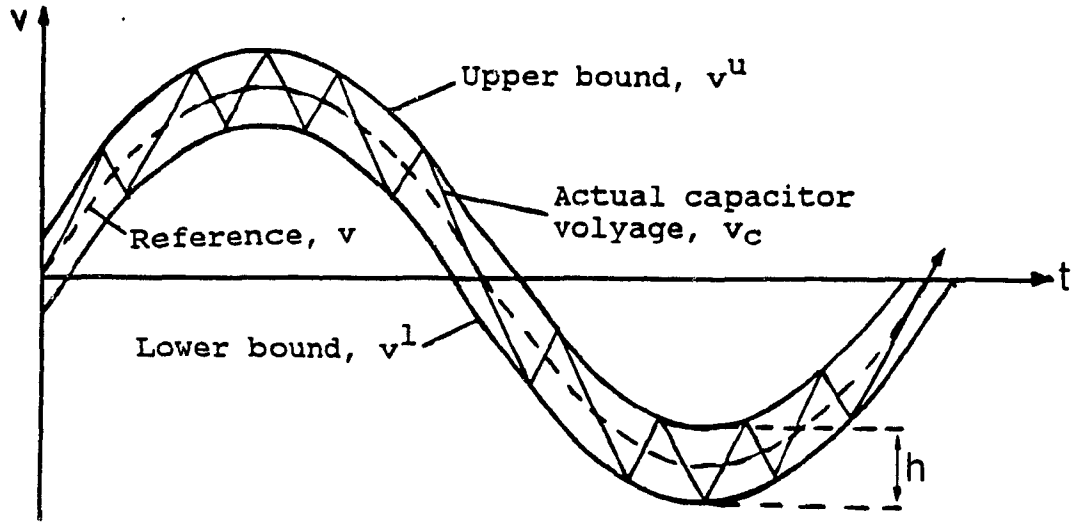


Fig.2.2 Delta Modulation Control Waveform.

2.2 THEORETICAL FORMULATION

Fig.2.3 shows the principal block diagram of Delta Modulated Converter for the "R" phase. Eqs. (2.1 - 2.5) are the simple basic equations applied to generate the voltage templates for the purpose of unity power factor operation.

However the power factor can be varied by varying the values of R and X in the control loop.

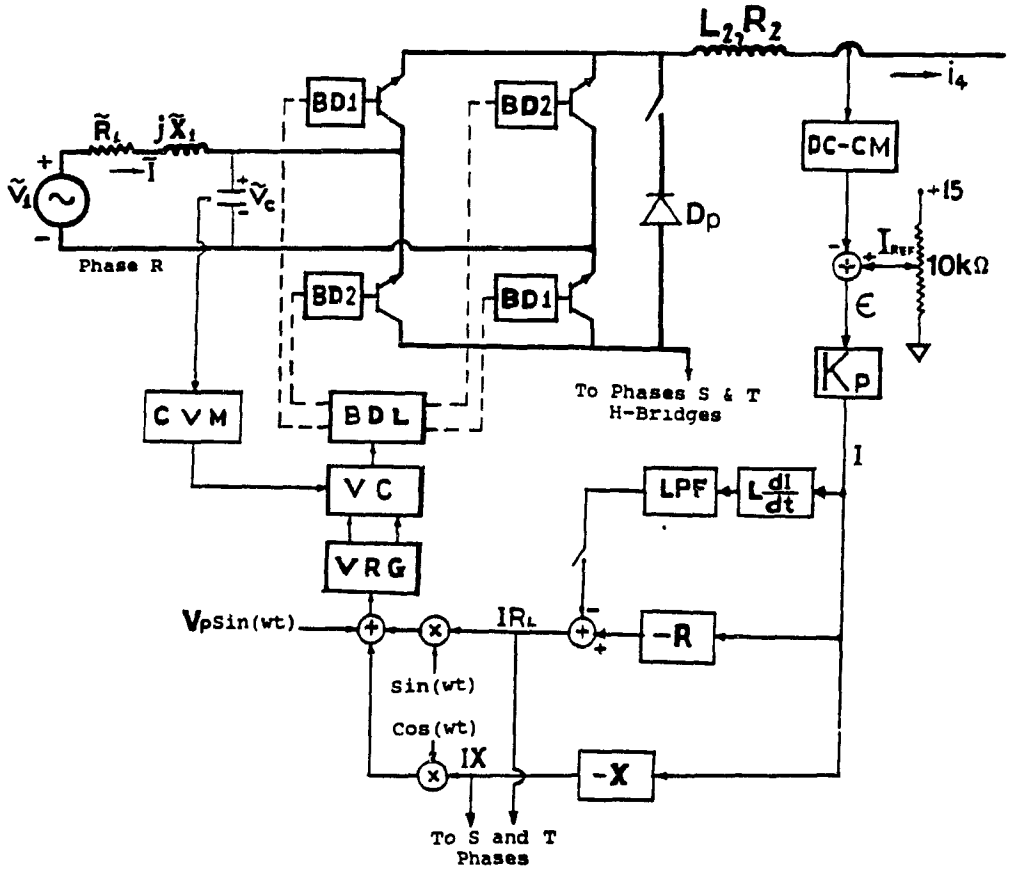


Fig.2.3 The Delta Modulation Controller for One Phase.

The capacitor voltage $v_c(t)$ can be expressed as:

$$v_c(t) = v_1(t) - i_1(t)R_1 - L_1 di_1(t)/dt \qquad (2.1)$$

where $v_1(t)$ is the a.c. source voltage, $i_1(t)$ is the a.c. source current, R_1 is a.c. source resistance and L_1 is the a.c. source leakage inductance.

The instantaneous a.c. source voltage is given by:

$$v_1(t) = V_p Sin(wt) \qquad (2.2)$$

where V_p is the peak phase voltage and w is the power angular velocity. At unity power factor, the a.c. source current is in phase with the a.c. source voltage such that it is expressed as:

$$i_1(t) = I_p(t)\mathrm{Sin}(wt) \qquad (2.3)$$

where $I_p(t)$ is the peak phase current (I_p may be a function of time during transients).

Hence, at unity power factor, eq.(2.1) becomes:

$$v_c(t) = (V_p - R_1 I_p(t) - L_1 dI_p(t)/dt)\mathrm{Sin}(wt) - X_1 I_p(t)\mathrm{Cos}(wt) \qquad (2.4)$$

where $X_1 = wL_1$, the a.c. source leakage reactance.

Eq. (2.4) can be simplified further to give eq. (2.5):

$$V_c(t) = V_{cd} - jV_{cq} \qquad (2.5)$$

where V_{cd} and V_{cq} are in phase and in quadrature components of the capacitor voltage respectively. At steady state the term $L_1(dI_p(t)/dt)\mathrm{Sin}(wt)$ disappears and the phasor diagram of the system is as shown in Fig.2.4.

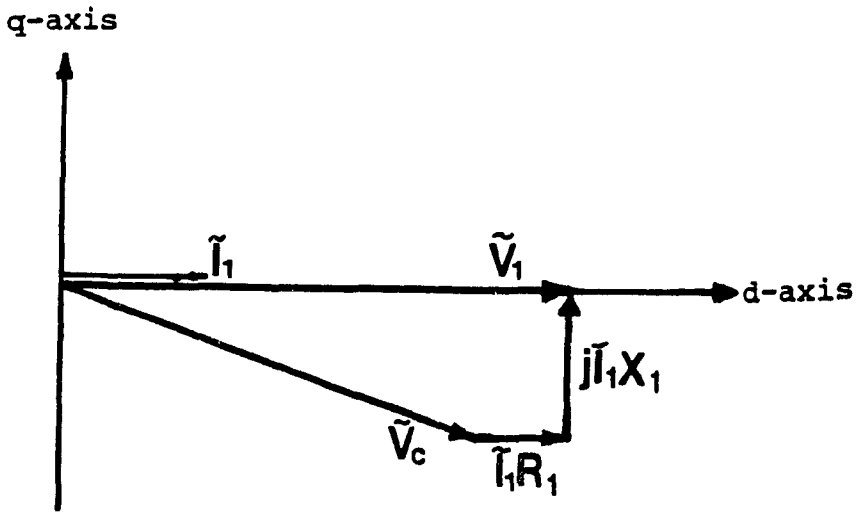


Fig.2.4 Phasor diagram for unity power factor operation.

From the phasor diagram it can be seen that power transfer is governed by δ, the angle between the a.c. source voltage and the capacitor voltage.

2.3 PRACTICAL IMPLEMENTATION

This section gives the details of hardware implementation of each block in Fig.2.3.

2.3.1 Voltage Template Derivation (VTD)

Fig.2.5 shows the circuit diagram of the three phase voltage template derivation circuit. The three phase voltage signals from the utility supply (through step down transformers) are passed through Band-Pass filters with phase shift compensation.

Fig.2.6 shows the circuit diagram for derivation of a.c. input parameters. The current signal, I, is the output of the d.c. current feedback block (see Fig.2.7). The a.c. input parameter output signals, R, X and LdI/dt are common to all three phases. These parameters were made variable for two purposes:

(i) To compensate the error in the current signal, I, since the current signal used in the control circuit is not derived from the a.c. power circuit as it has been shown in eq.2.1.

(ii) To have the possibility of varying the power factor.

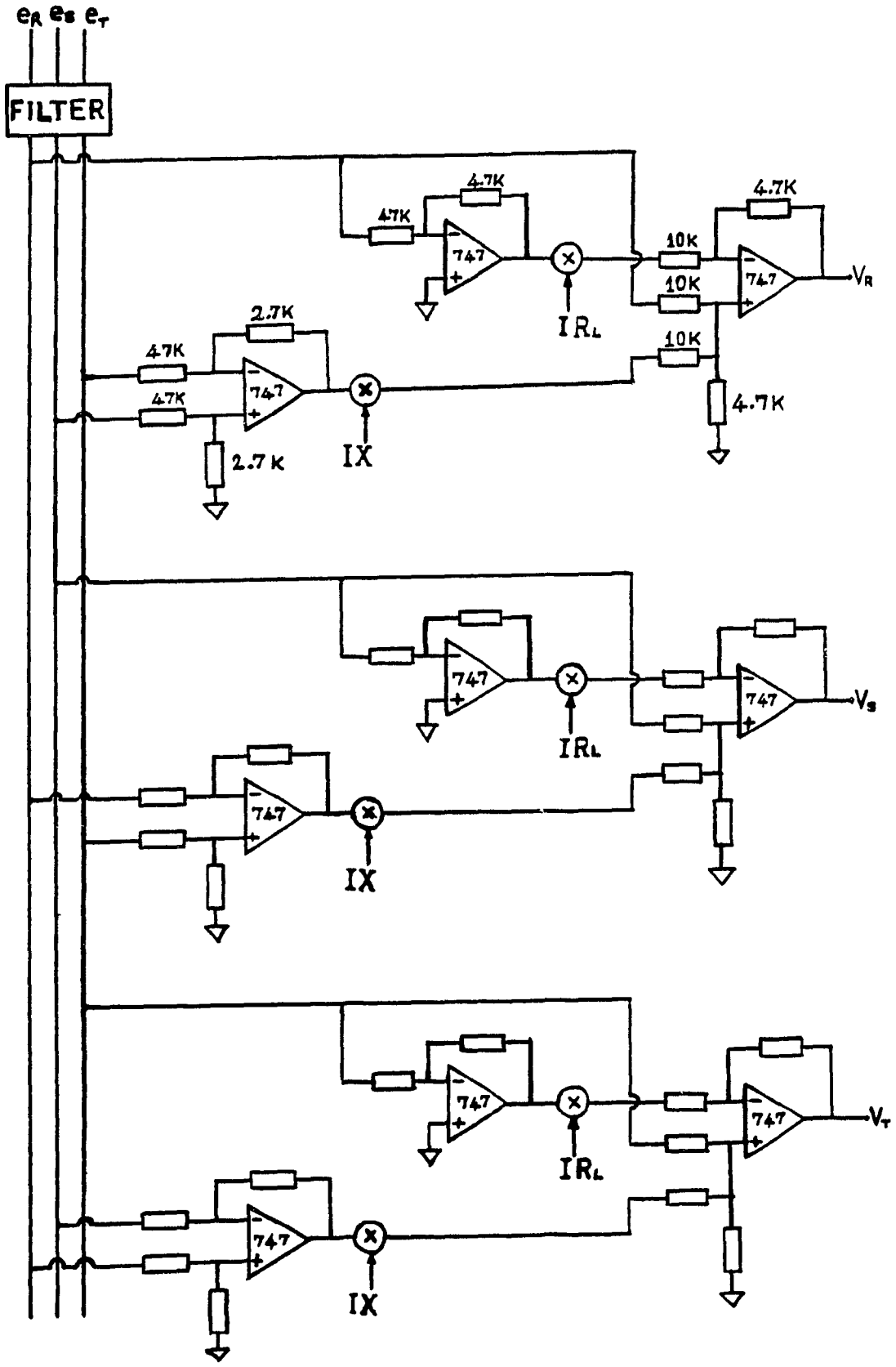


Fig.2.5 Circuit Diagram for Voltage Template Derivation.

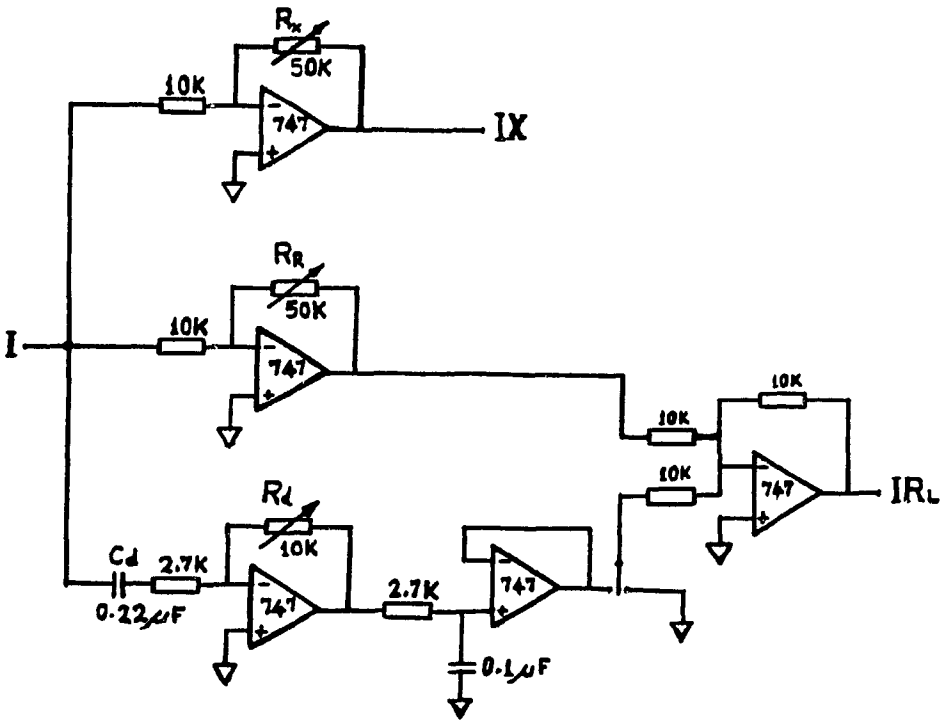


Fig.2.6 Circuit diagram for derivation of a.c. input parameters.

2.3.2 D.C. Current Feedback

The circuit diagram for the d.c. current feedback block is shown in Fig.2.7. The d.c. current measurement adopted, used a Hall Effect Current Transducer. The electrical characteristics of the transducer can be found in [15,33]. Since the device is a flux detector, it can measure d.c. currents. The frequency response is zero to 100kHz. The measured d.c. current is compared with the reference. The current error is multiplied by the proportional control gain K_p. The output signal, I, is fed to the a.c. input parameters' blocks, R, X and LdI/dt (see Fig.2.6).

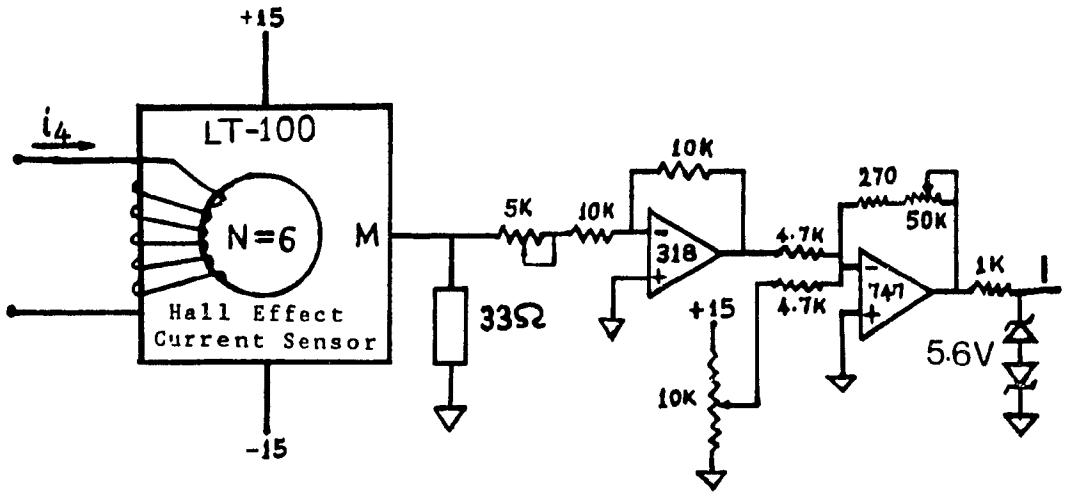


Fig.2.7 Circuit Diagram for D.C. Current Feedback.

2.3.3 Voltage Reference Generator (VRG)

As mentioned before, the capacitor voltage is required to vary within specified limits (Voltage Hysteresis Window "h"). That is there was a need of a circuit which can change the voltage template into two signals, the Upper and Lower reference bounds. Fig.2.8 shows the circuit diagram for one phase. This circuit produces the Upper and Lower reference bounds with hysteresis and offset adjustments.

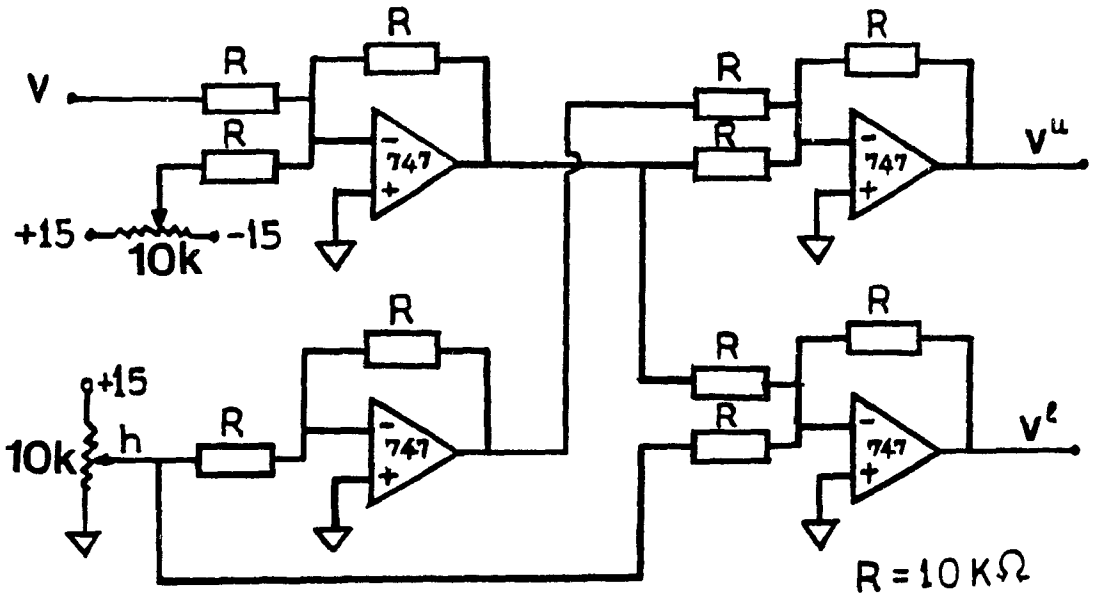


Fig.2.8 Voltage Reference Generator (VRG).

2.3.4. Capacitor Voltage Measurement (CVM)

The capacitor voltage measurement technique adopted, used an Opto-coupler link for electrical isolation. Here the Opto-isolator measurement method was used instead of the available Hall-Effect voltage sensors because it was found that the later has a very narrow band width. A 10000:36 Ohm resistive voltage divider was connected across the capacitor. The voltage across the 36 Ohm resistor was used to represent the capacitor voltage signal. This approach enabled high bandwidth components to be used which were capable of following fast changes in the instantaneous capacitor

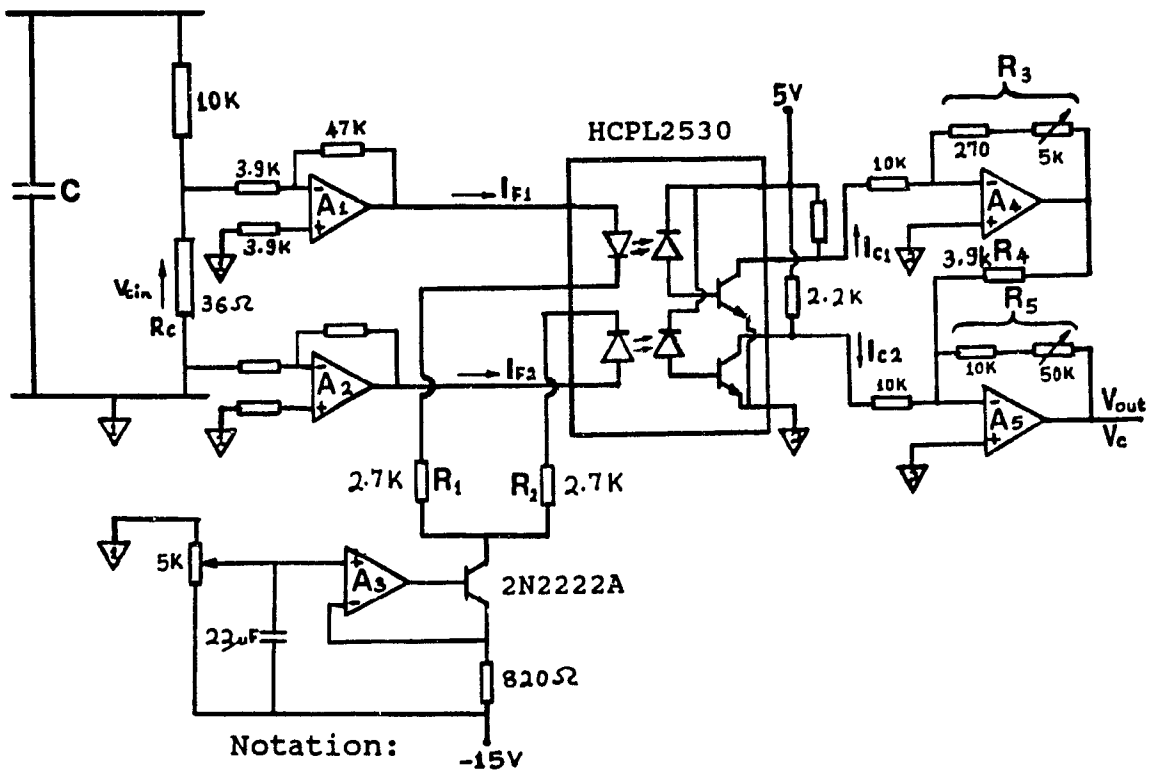
voltages superimposed on a power frequency fundamental. A true d.c. isolated voltage signal was thus obtained.

This section gives the principle of operation of the capacitor voltage measurement circuit and assesses its performance.

2.3.4.1 Circuit Operation

The Opto-coupler circuit used is given in Fig.2.9. The specifications for the HCPL2530 Opto-couplers are given in Appendix A [44].

The circuit acts as a differential isolation amplifier. The operation principle relies on the existence of an operating region where the gain increment in one of the pair of optically coupled isolators can be approximately balanced by a gain decrement in the second opto-isolator. As I_{F1} increases in the first opto-isolator, I_{F2} decreases in the second by an equal amount. The gain increment caused by increase in I_{F1} will be approximately balanced by the gain decrement caused by decrease in I_{F2}. The constant current source biases each input LED an equal quiescent current. R1 and R2 can be chosen to suit any desired input voltage range.



Notation:

A_1, A_2, A_3 : LM318 High Speed Amplifiers
A_4, A_5 : TL072CP Low Noise Amplifiers
I_{F1}, I_{F2} : Opto-coupler Diode Currents
I_{C1}, I_{C2} : Opto-coupler Transistor Currents
R_c : Capacitor Voltage Measurement Resistor

: Neutral Point of a Phase

: Control Circuit Ground

Fig.2.9 Opto-isolator Link for Capacitor Voltage Measurement.

At the output, the operating amplifier A_4 and A_5 force the output voltage v_{out} $(=v_c)$ to be directly proportional to the difference between I_{c1} and I_{c2} according to equation (2.6).

$$V_{out} = R_5(I_{c1}R_3/R_4 - I_{c2}) \qquad (2.6)$$

The zero adjustment potentiometer, R_3, allows v_c to be tuned to zero when v_{cin} is zero.

2.3.4.2 Three Phase Voltage Measurement

Three Opto-coupler circuits were required to measure the capacitor voltages in all three phases. Since the three phases in the power circuit are floating, then it was necessary to use three isolated power supplies for the three phase Opto-coupler input stage circuits (primaries).

2.3.4.3 Choice of Amplifier

The bandwidth of the Opto-coupler voltage measurement circuit was limited by the operational amplifiers used. The circuit was required to measure signals in the 5.0 - 20kHz region. The constraints were the speed and noise level of the amplifiers. High speed amplifiers are noisy, while less noisy amplifiers are relatively slow. In order to compromise with the two constraints, high speed amplifiers were used at the input stage while low noise and relatively high bandwidth amplifiers were used at the output stage.

2.3.4.4 Gain and Drift Considerations

This circuit is sensitive to temperature fluctuations. Typical temperature performance quoted for the circuit is **Offset drift = -1.6mV/C** [45].

Furthermore the Opto-couplers suffer from non-linearity problem. The change in gain can be compensated by a thermistor in either the input or output circuit. Typically, R_5 can be replaced by a positive thermistor.

Amplifier A_5 gives the offset drift compensation circuit with further amplification.

This circuit offers a simple and cheap means to optically isolate an analogue signal. As such the circuit was deemed suitable for achieving an isolated capacitor voltage signal.

2.3.4.5 Output Waveforms

Fig.2.10a and 2.10b show the photographs of the overall and expanded section of the capacitor voltage waveforms. They show that the measured signal is clean and sharp with little interference caused by the high speed switching of the power devices.

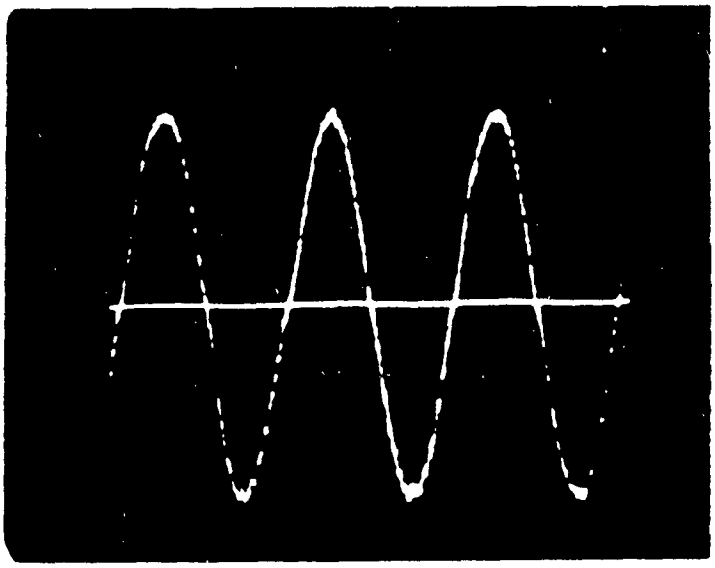


Fig.2.10a Instantaneous capacitor voltage, v_c.

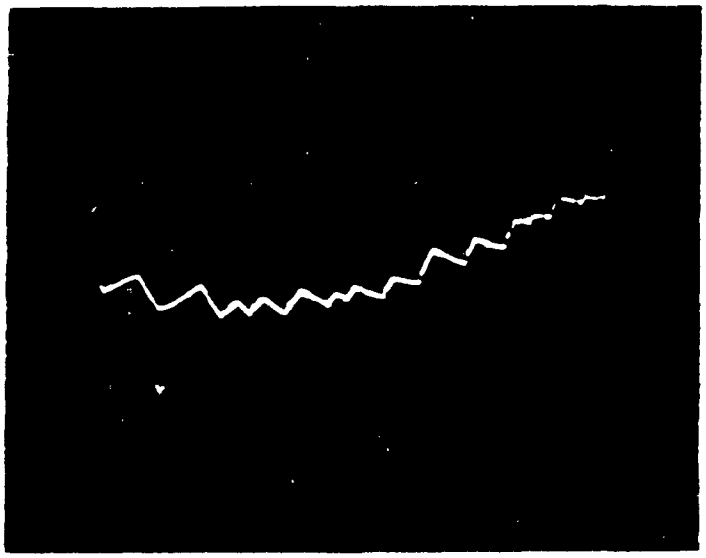


Fig.2.10b Expanded time scale of Fig.2.10a.

2.3.5 Voltage Comparison (VC)

The voltage comparison was achieved using analogue techniques to reduce delay times in the capacitor voltage feedback loop. The purpose of the voltage comparison circuit is to perform two functions:

(i) Comparison of the capacitor voltage signal with the two voltage reference bounds V^u and V^l. The logic output signals "V_r" and "V_l" are then interpreted by the base drive logic circuitry to switch the power transistors appropriately.

(ii) Comparison of the voltage reference bounds V^u and V^l with zero to generate interlock signals m1 (T_1 transistor group modulate signal) and m2 (T_2 transistor group modulate signal).

2.3.5.1 Circuit Operation

Fig.2.11 shows the circuit diagram used in voltage comparison. The input signals are the upper and lower bound reference voltages coming from the VRG circuit (see Fig.2.8) and the inverted actual capacitor voltage signal, $-v_c$ coming from the CVM circuit through inverting amplifier.

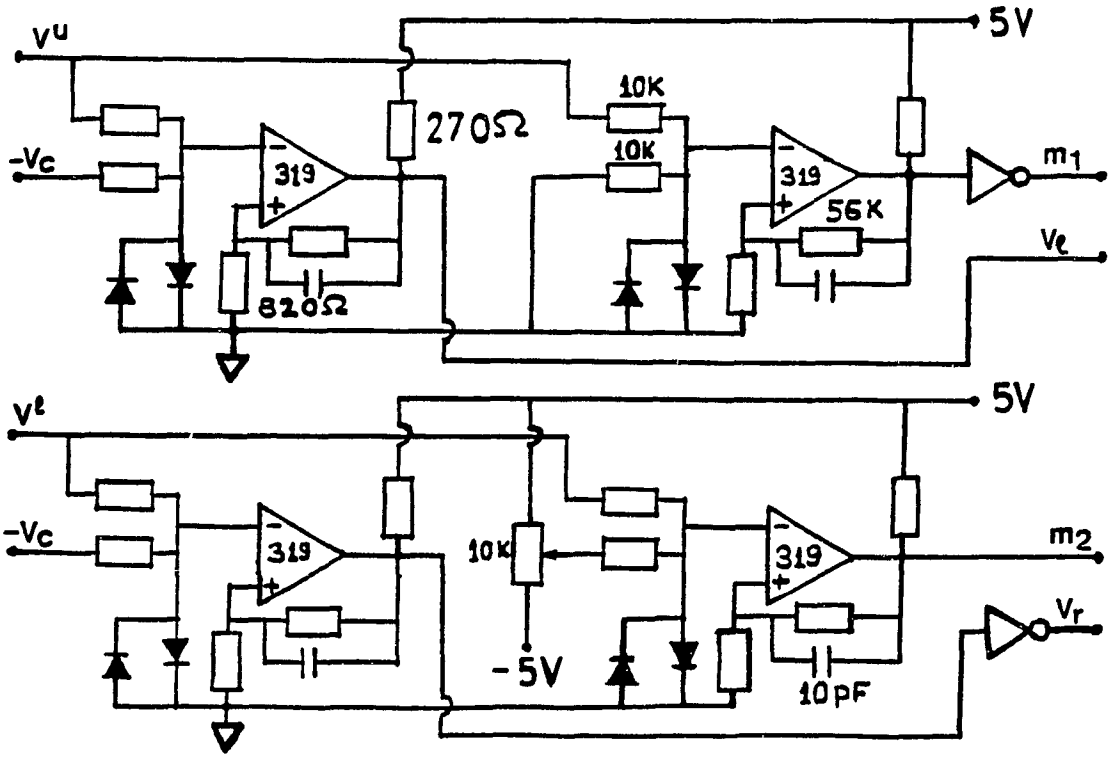


Fig.2.11 Voltage Comparison Circuit (VC).

The output signals "V_r" and "V_l" are the normal signals to the base drive logic to raise and lower the level of the capacitor voltage respectively.

However, since the converter is the current source, then the d.c. current should always have a path through the H-bridges. This condition is fulfilled by the output signals

m1 and m2. The functions of m1 and m2 are described with the help of Fig.2.12. It can be seen that m1 (T_1 transistor group modulate signal) enables T_2 transistor group when the upper voltage bound is positive. While m2 (T_2 transistor group modulate signal) enables T_1 transistor group when the lower voltage bound is negative. During overlap period, the d.c. current is freewheeled across the H-bridge of one phase, and it may flow in the other two phases. However this circuit has to be modified for the reasons explained in section 2.3.7.

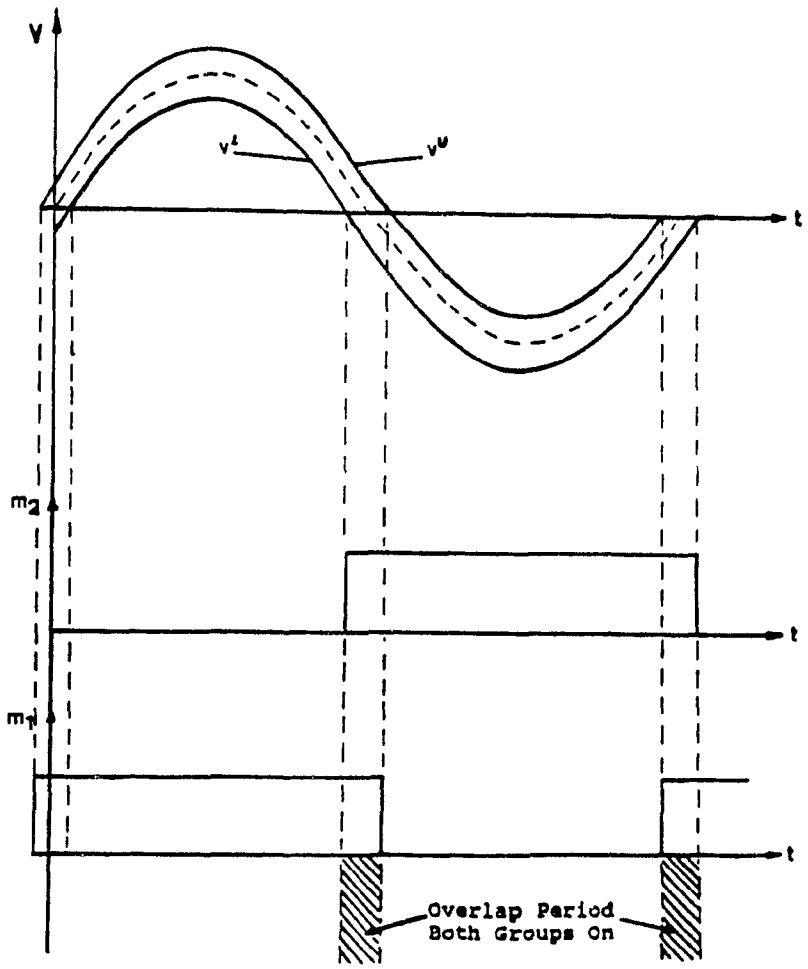


Fig.2.12 Generation of m1 and m2 signals.

2.3.6 Base Drive Logic (BDL)

This circuit ensures that the d.c. current has a continuous path across the H-bridge of any phase. Also there is an overlap of one clock period between turning on of the incoming transistor group and turning off of the outgoing transistor group. The clock also controls the maximum switching frequency.

Fig.2.13 shows the circuit for base drive logic. The details for the design of base drive units can be found in [15,16,33].

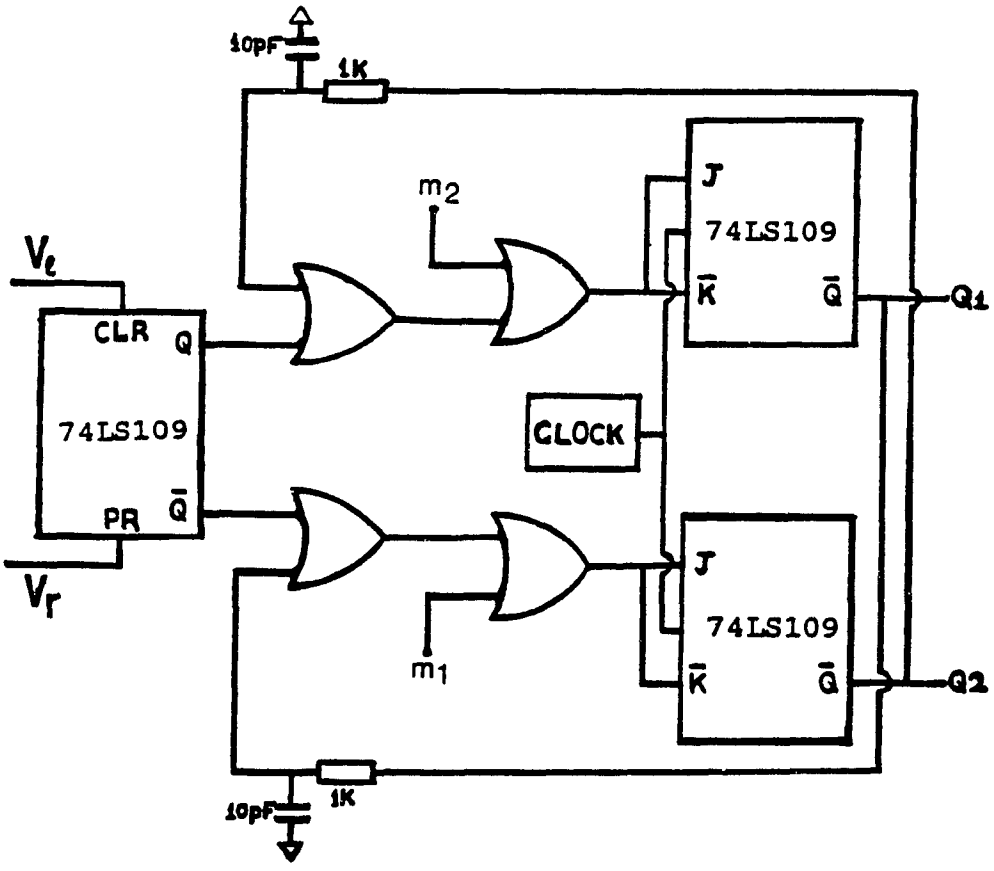


Fig.2.13 Base Drive Logic Circuit (BDL).

Fig.2.14 shows the transistor switching logic signals in relation to the capacitor voltage variation within the upper and lower voltage reference bounds. It also shows m1 and m2 signals in relation to the upper and lower voltage reference bounds.

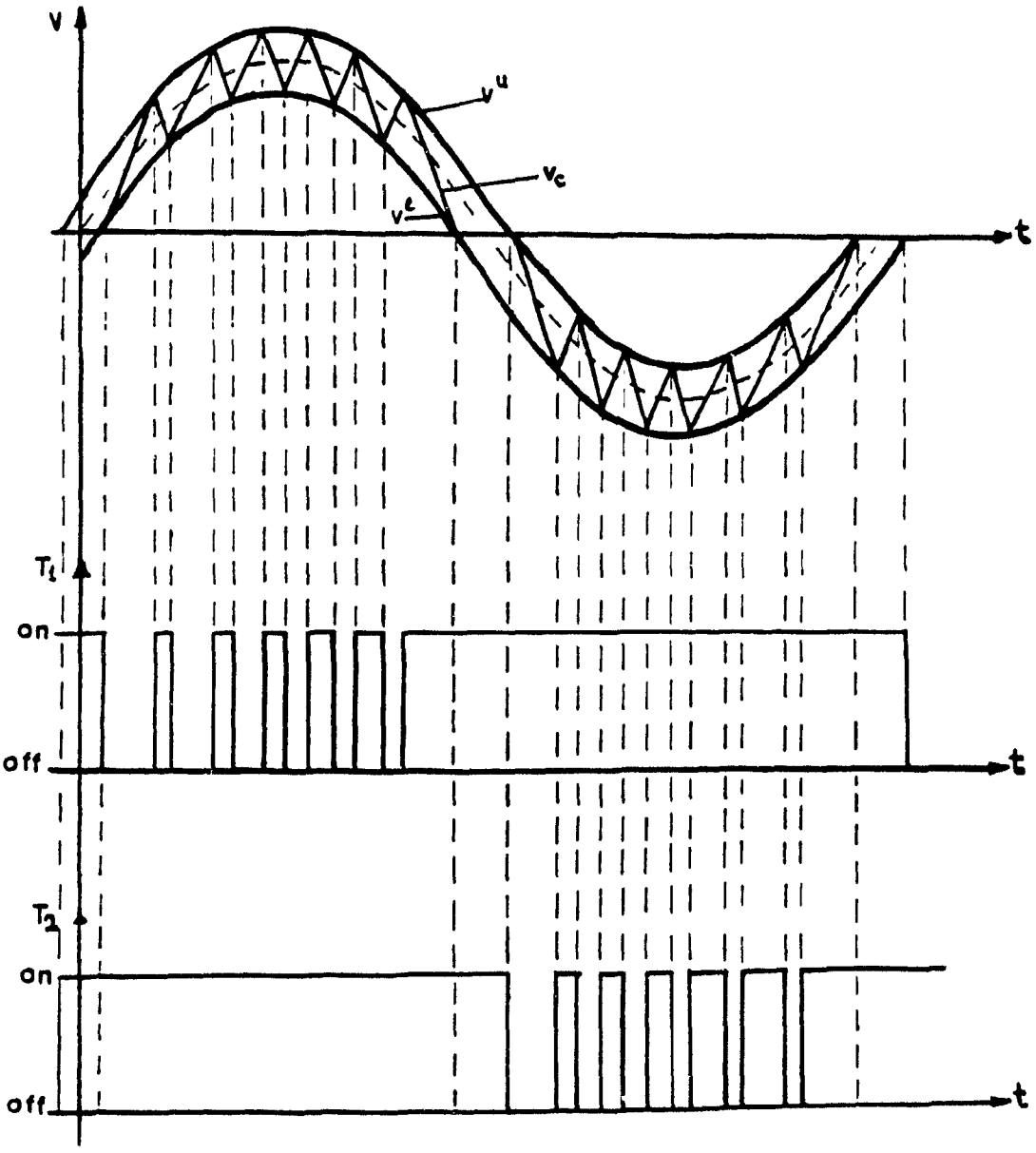


Fig.2.14 Transistor Switching Logic Signals.

2.3.7 Modified Voltage Comparison (MVC)

With the voltage comparison circuit shown in Fig.2.11, it was found that the overlap period causes distortion of the capacitor voltage and the a.c. source current. In order to minimize distortion, the voltage comparison circuit had to be modified. In the modified circuit, the signals m1 and m2 were taken out. In order to ensure the d.c. current continuity, the clock period in the base drive logic was increased so as to offer enough short time overlap periods between switching instants of T_1 and T_2 transistor groups. Fig.2.15 shows the modified voltage comparison circuit. The output signals "V_r" and "V_l" are fed to the base drive logic circuit and function as explained in section 2.3.5.

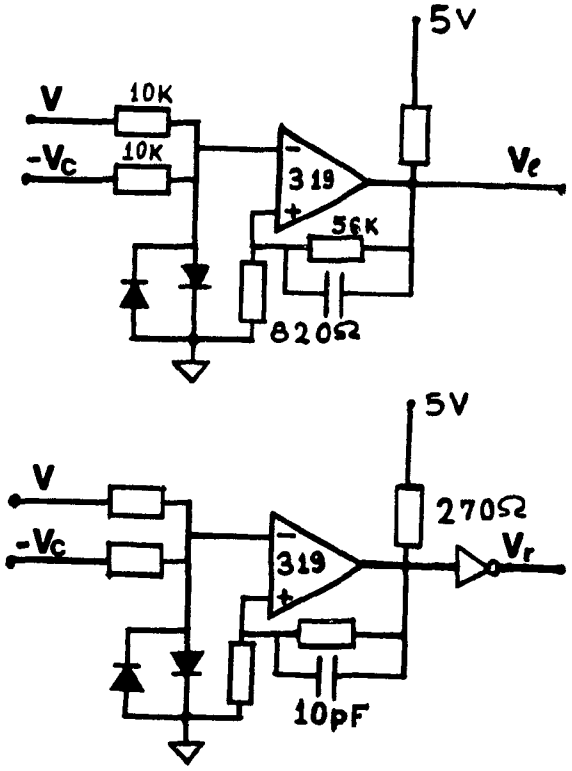


Fig.2.15 Modified Voltage Comparison Circuit (MVC).

2.3.8 Modified Base Drive Logic (MBDL)

The base drive logic modification was done in order to match with the modified voltage comparison circuit. Fig.2.16 shows the modified base drive logic circuit. In this circuit there are only two input signals coming from the MVC circuit, "V_r" and "V_l". The d.c. current continuity is assured by short time overlap between "ON" state of incoming transistor group and "OFF" state of outgoing transistor group. The short time overlap periods are equal to one clock cycle which is about 10μsec.

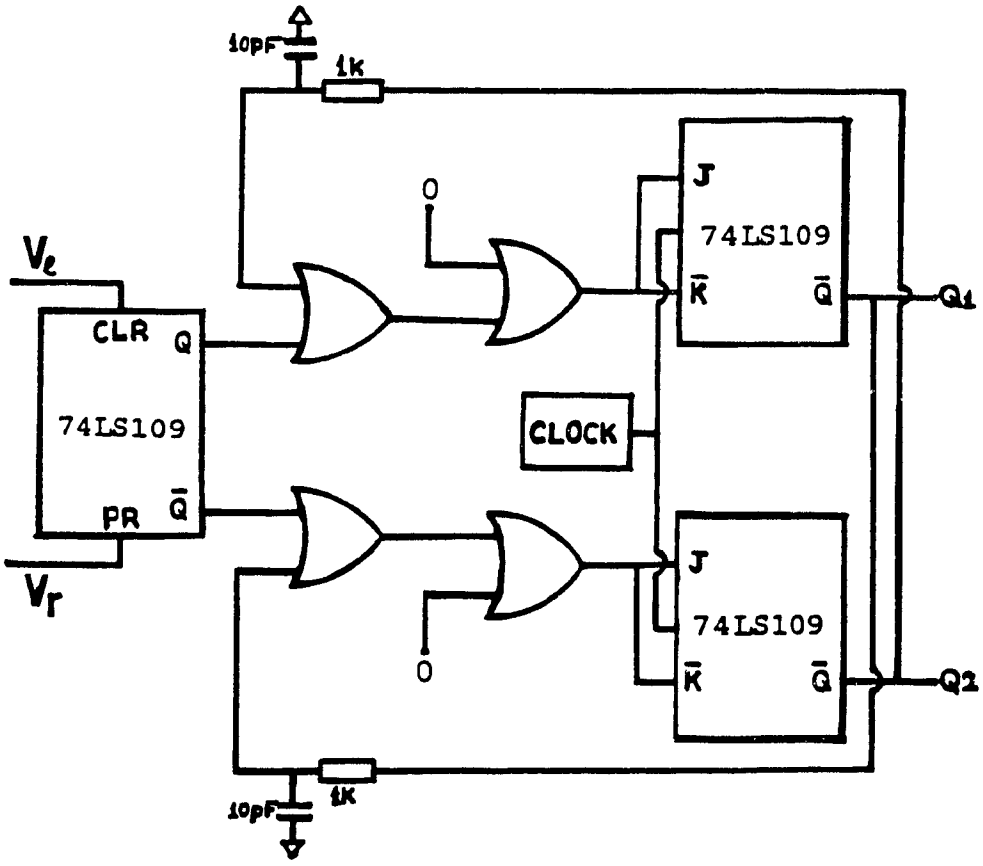


Fig.2.16 Modified base drive logic circuit (MBDL).

Fig.2.17 shows the transistor switching logic signals in relation to the capacitor voltage variation within the upper and lower voltage bounds. The short time overlap periods are not shown in Fig.2.17.

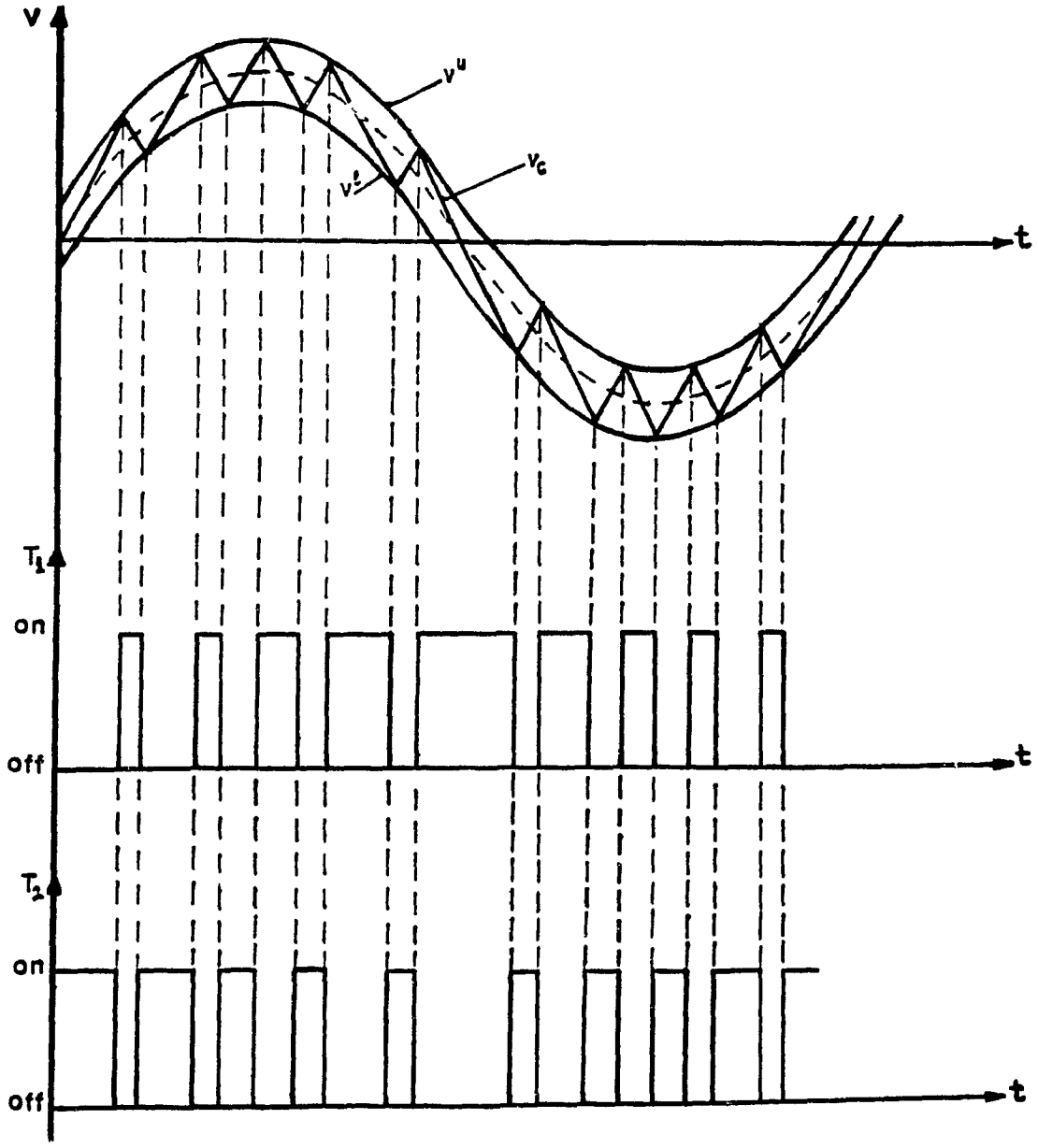


Fig.2.17 Transistor Switching Logic Signals.

2.5 SUMMARY

This chapter described the Delta Modulation Control strategy used in achieving near sinusoidal a.c. input currents at unity power factor, with a possibility of leading power factor.

The overall Delta Modulation Control scheme adopted was described. Circuit implementation of each stage of the control scheme was explained. An isolated d.c. representation of the capacitor voltage was achieved by using a resistive potential divider connected in parallel to the capacitor and an Opto-coupler circuit. Voltage comparison and base drive logic circuits were described and their practical implementation were given.

Physical construction of the control circuits are given in the photographs in appendix C.

The next chapter presents the circuits of power switch modules.

CHAPTER III

THE POWER CIRCUIT

The power circuit form the central hardware core of the converter. The original topological dual design and details are given in [16,33]. However it was necessary to carry out some re-arrangements in order to suit the present topology. In the implementation, care was taken in the lay out of the circuit elements for easy trouble-shooting and repairs. Printed circuit board technology was adopted wherever possible. Moreover modularity and interchangeability of circuit boards was stressed. The power switch modules consist of:

1. Three single phase bipolar transistor bridges
2. The snubber circuits
3. The base drive (BD) units

It is not the purpose of this chapter to repeat what is found in [16,33]. Readers are advised to refer to these references for details of the design.

Since the present circuit topology is different from the previous ones, this chapter has the purpose to present the complete power circuit diagram of this topology. Researchers following this work may benefit from the complete documentation of this converter topology for further development and improvement. Details of the base drive circuitry can be found in [15,16,33].

3.1 THE THREE PHASE CONVERTER POWER CIRCUIT

The power circuit used is shown in Fig.3.1 excluding the snubber circuits.

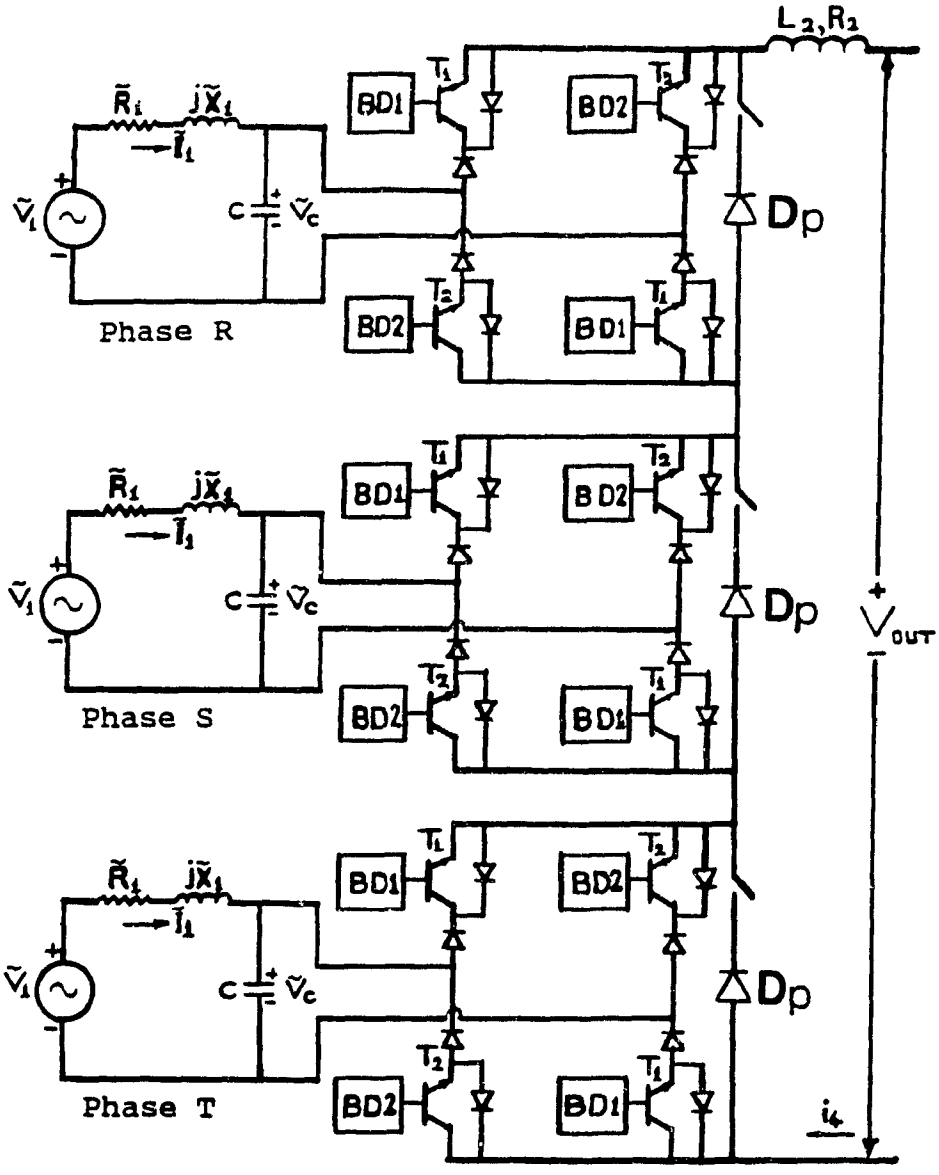
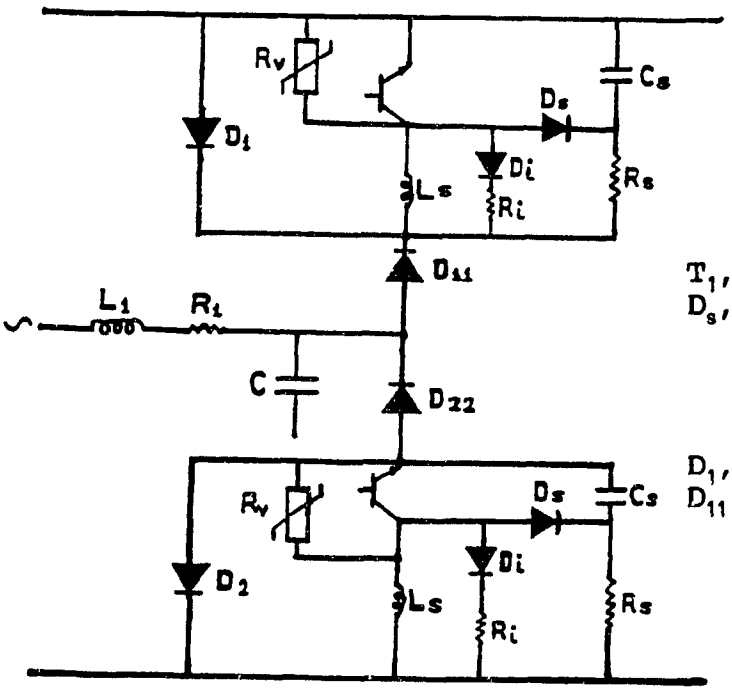


Fig.3.1 Power Circuit for the Three Phase Converter.

Each base drive unit (BD), commands one of the transistors of the H-bridges. The "common emitter" transistors' base drive units are fed by the same power supplies, while the other transistors' base drive units are fed by independent power supplies. For each phase, the base drives with the same number (BD1 or BD2) receive the same signal from the base drive logic circuit.

3.2 THE SNUBBER PROTECTION

The snubber circuits protect the power devices against high current and voltage slopes during switching. Fig.3.2 shows the snubber circuit used.



Notation:

T_1, T_2	: MJ10015
D_s, D_i	: MR854
C_s	: 0.051μF
R_i	: 3.3Ω,3W
R_s	: 68Ω,2W
L_s	: T80-40, 7t
D_1, D_2	: 40HFL60SO2
D_{11}, D_{22}	: 40HFL60SO2
R_v	: Varistor

Fig.3.2 The Snubber Protection for One leg of Phase "R" H-bridge.

3.3 THE BIPOLAR TRANSISTORS

The switching devices used in the converter are Darlington Bipolar Transistors. Fig.3.3 shows the internal circuit arrangement of one of the transistors and its data sheets are given in Appendix B [45].

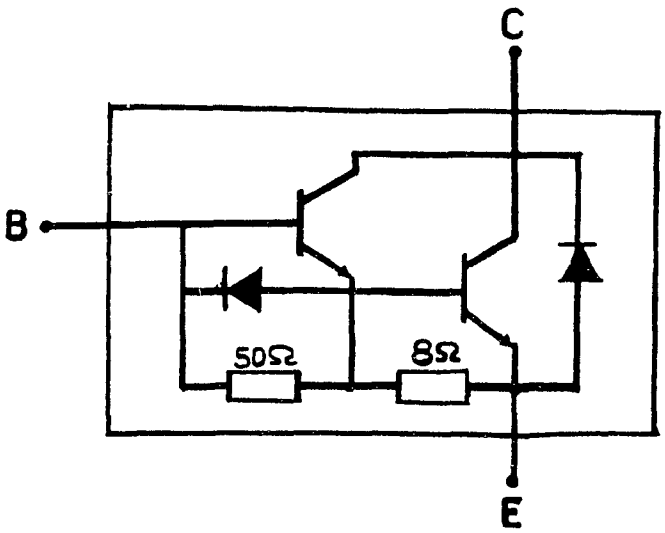


Fig.3.3 The MJ10015 Power Transistor.

3.5 SUMMARY

The circuits of the power switches and snubber protection have been described. Physical constructions of the power circuit modules are shown in the photographs in appendix C.

The next chapter will describe briefly the modes of operation of the converter and range of parameter values used during the tests.

CHAPTER IV

MODES OF OPERATION AND PARAMETER CONSTRAINTS

Chapter II, contains a detailed description of the principles and circuit implementation of Delta Modulation Control. In Chapter III, the construction of the electronic power switch modules, the snubber protection circuits and the base drive circuits have been described. The integration of all these components' parts form the Delta Modulated Converter. Since this topology is at its earliest stage, this chapter is devoted to give detailed operating modes and parameter constraints. However, since the system is a topologically dual of the Controlled Current PWM Converter, for better understanding, the reader is advised to consult [15,16,33]. In this chapter two modes of operation of the converter will be described. First, the inter-phase diodes are connected, where power can only flow from a.c. side to d.c. side. The second operating mode is when the inter-phase diodes are disconnected, where power may flow back to the a.c. side from the d.c. side.

In Chapter II, two alternative comparison and logic circuits were given and discussed. For the reasons already explained, this chapter presents operating modes of the converter using the "Modified" VC and BDL circuits only.

The hints on the range of values of the a.c. capacitor, a.c. source resistor, a.c. source inductor, K_p

and d.c. inductor which were used during the test of the converter are presented. The range of parameter values were predicted by computer simulations which are not included in this thesis. The parameter ranges given here are based on experimental tests. Proper parameter dimensioning for a desired rating of the converter can be done after exhaustive analytical and experimental evaluation of the converter.

4.1 OPERATION WITH THE INTER-PHASE DIODES

With the inter-phase diodes in the circuit, the system can only be operated as a rectifier. Inverter operation requires reversing the d.c. voltage which will forward bias the inter-phase diodes making the whole operation impossible. Figure 4.1 shows the instantaneous waveforms of the capacitor voltage, v_c, the upper and lower voltage reference bounds, V^u and V^l, and the pre-filtered d.c. voltage, V_t. In the instantaneous d.c. voltage waveform, the small negative voltage pulses are due to forward drop of the single phase H-bridge.

The two switching periods, "Voltage Raise" and "Voltage Lower" are best explained with the aid of Fig.4.2, 4.3 and 4.4. For reference, positive half cycle of the sinusoidal wave is taken. Fig.4.2 and 4.3 show the conducting transistor groups during "Voltage Raise" and "Voltage Lower" periods respectively. Fig.4.4 shows a small portion of the capacitor voltage in relation to the upper and lower bounds.

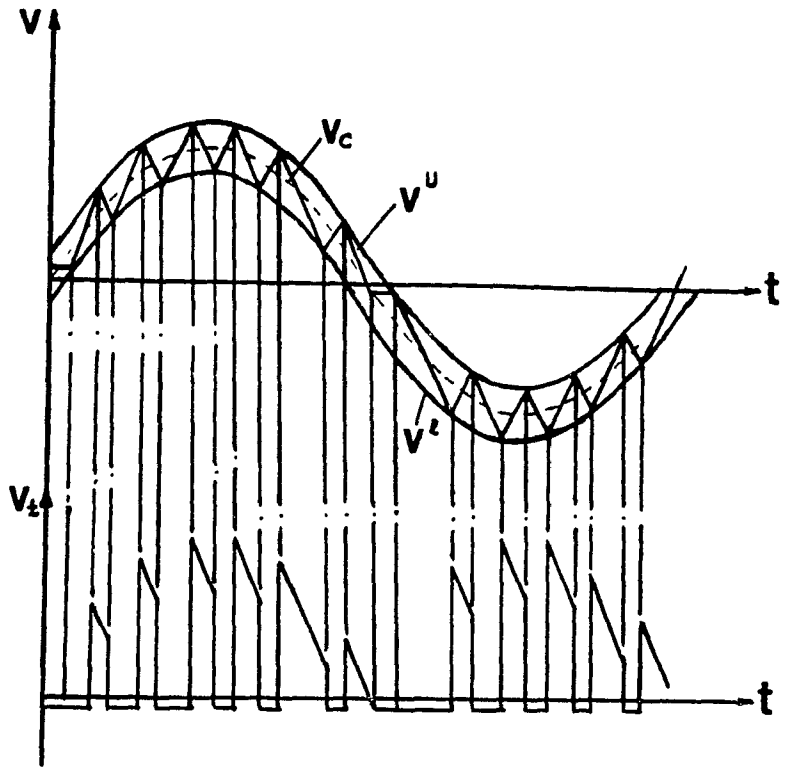


Fig.4.1 Operation with the inter-phase diodes.

(i) Voltage Raise time period, δt_1

During this period transistor group T_2 is conducting and the capacitor is charged to raise its instantaneous voltage from point A to point B as shown in Fig.4.4. At the same time V_t is as shown by dotted lines. As such the inter-phase diode is forward biased and conducts the d.c. current.

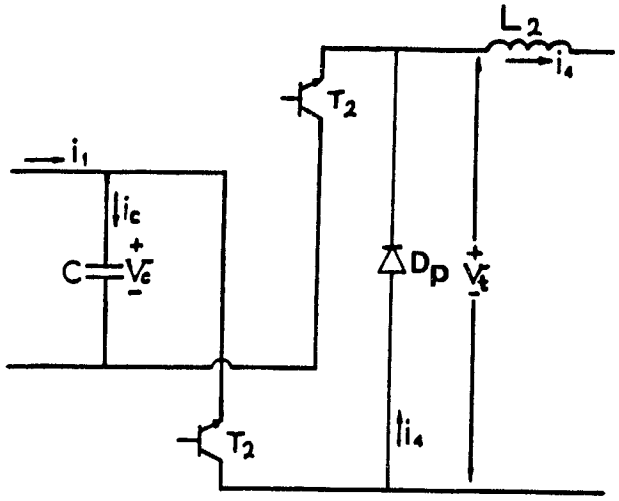


Fig.4.2

Transistor group T_2 conducting, time period δt_1.

(ii) Voltage lower time period, δt_2

Time period δt_1 ends at point B where time period δt_2 starts. During this period transistor group T_1 is conducting and the capacitor is discharged to lower its voltage from point B to point C. The inter-phase diode is reverse biased and the d.c. current follows T_1 transistor group path and power is transferred from a.c. side to d.c. side. At point C another cycle starts.

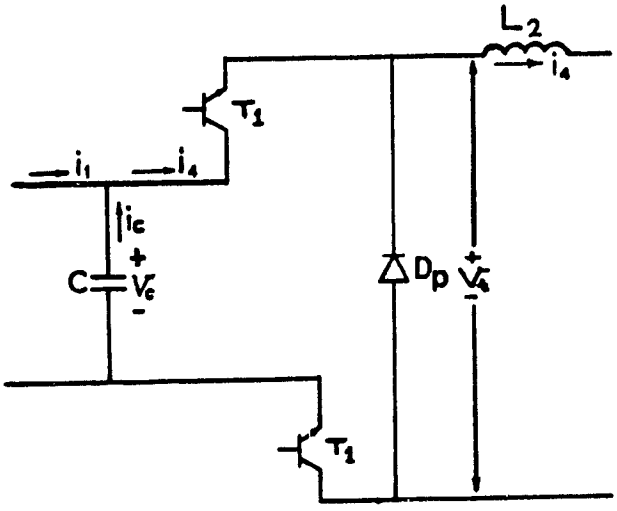


Fig.4.3

Transistor group T_1 conducting, time period δt_2.

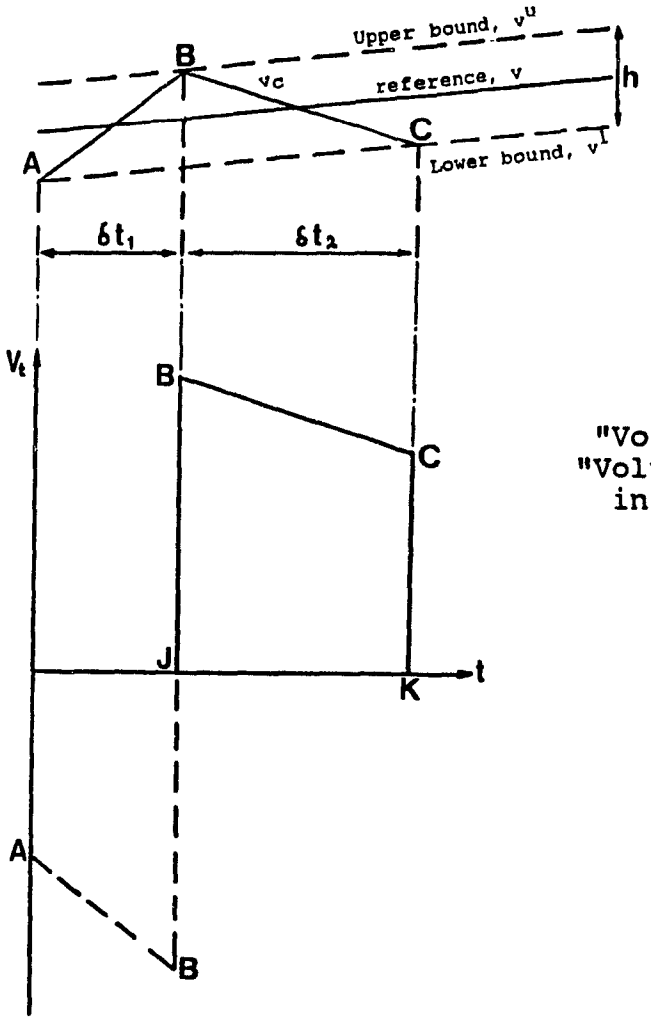


Fig.4.4

"Voltage Rise" and "Voltage Lower" periods in relation to the capacitor and d.c. voltage.

During negative half cycle the switching states of T_1 and T_2 explained in (i) and (ii) are reversed. As it can be seen in Fig.4.1, for large voltage window, presence of the inter-phase diodes introduce a dead zone of the capacitor voltage around zero. This situation causes distortion of both, capacitor voltage and a.c. source current. The dead zone as well as distortions can be suppressed by reducing the voltage window. A voltage window of about 2.5% of the peak capacitor voltage gives almost ideal results.

4.2 OPERATION WITHOUT INTER-PHASE DIODES

When the inter-phase diodes are out of the circuit, the system can be operated as a rectifier as well as an inverter. Inverter operation requires reversing the d.c. voltage. This thesis presents tests results for rectifier modes of operation only. Fig.4.5 shows the instantaneous waveforms of the capacitor voltage, v_c, the upper and lower voltage reference bounds, V^u and V^l, and the d.c. voltage, V_t.

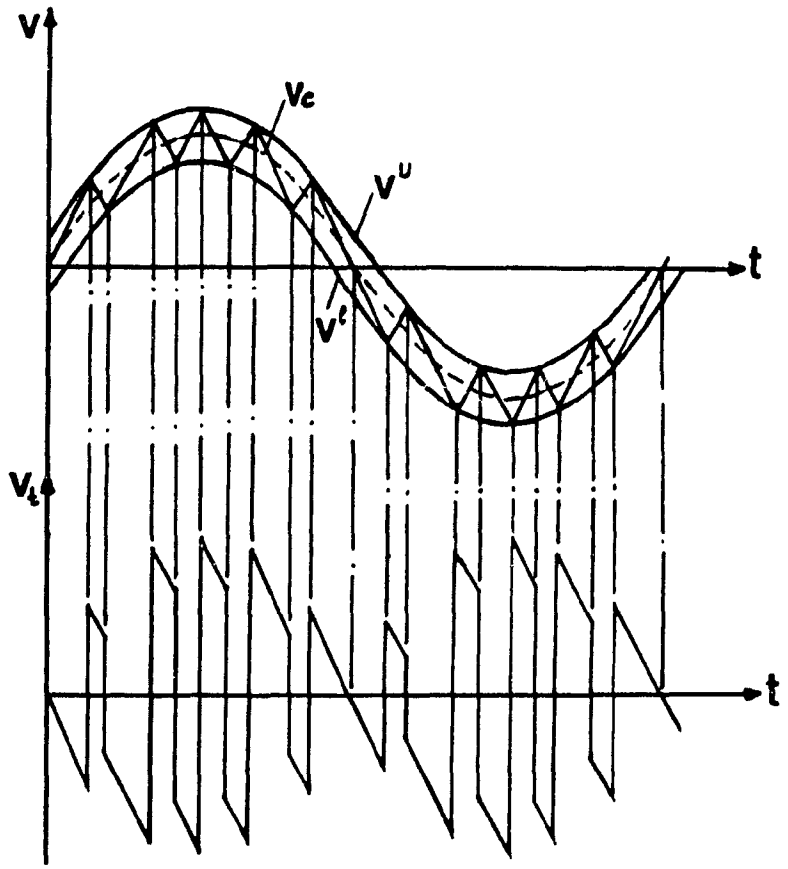


Fig.4.5 Operation without the inter-phase diodes.

The two switching periods, "Voltage Raise" and "Voltage Lower" are explained with the help of Fig.4.6, 4.7 and 4.8. Positive half cycle of the sinusoidal wave is taken as reference. Fig.4.6 and 4.7 show the conducting transistor groups during "Voltage Raise" and "Voltage Lower" periods respectively. Fig.4.8 shows a small portion of the capacitor voltage in relation to the upper and lower voltage bounds.

(i) Voltage Raise time period, δt_1

During this period transistor group T_2 is conducting and the capacitor is charged to raise its voltage from point A to point B as shown in Fig.4.8. At the same time V_t is as shown in figure 4.8. As a result the a.c. source and the d.c. link currents are charging the capacitor to raise its voltage up to the point B. In this case if it happens that the d.c. current is higher than the peak a.c. source current, then some power can be returned to the a.c. side during this period.

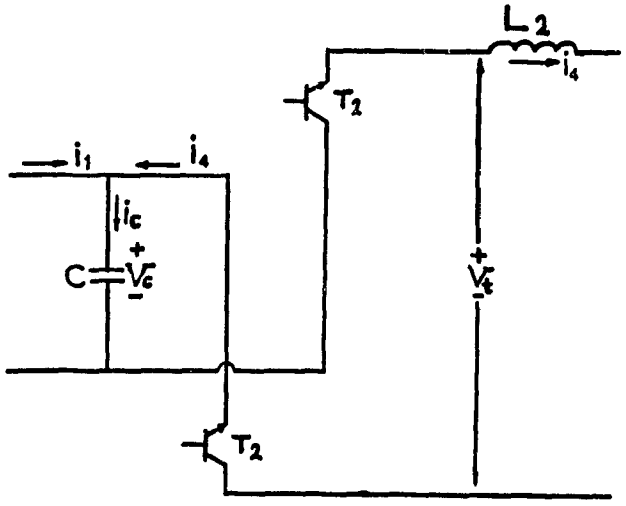


Fig.4.6

Transistor group T_2 conducting, time period δt_1.

(ii) Voltage lower time period, δt_2

Time period δt_1 ends at point B where time period δt_2 starts. During this period transistor group T_1 is conducting and the capacitor is discharged to lower its voltage from point B to point C. The d.c. current follows T_1 transistor group path. Meanwhile power is transferred from a.c. side to d.c. side. Another switching cycle starts at point C.

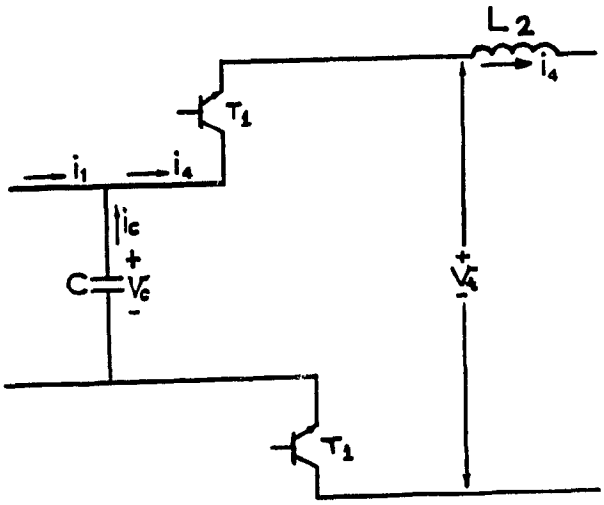


Fig.4.7

Transistor group T_1 conducting, time period δt_1.

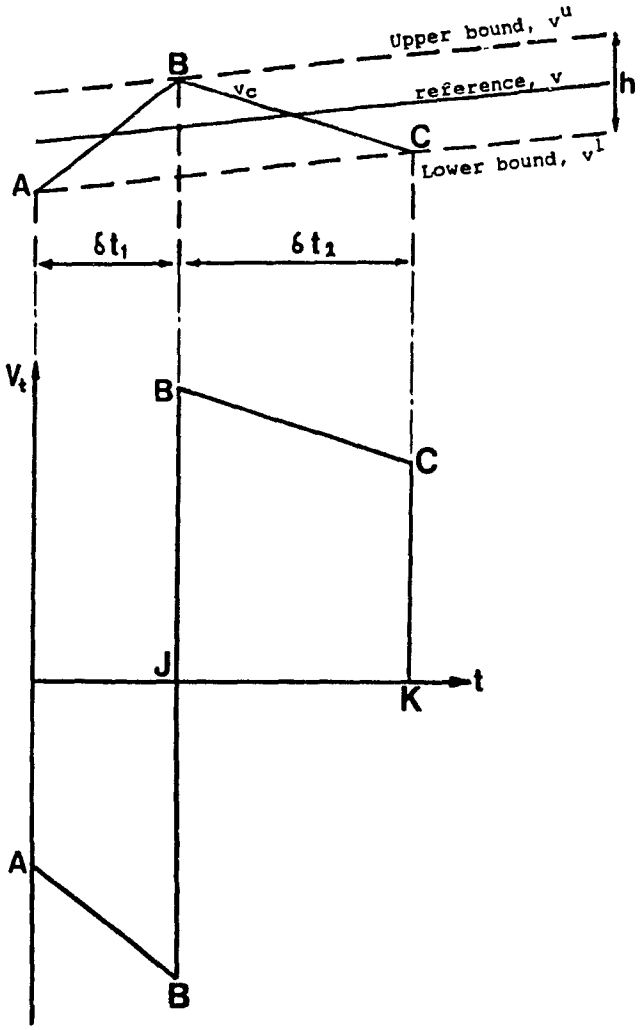


Fig.4.8

"Voltage Rise" and "Voltage Lower" periods in relation to the capacitor and d.c. voltage.

During negative half cycle the switching states of T_1 and T_2 explained in (i) and (ii) are reversed.

As it can be seen in Fig.4.5, absence of the inter-phase diodes gives no chance of dead zone of the capacitor voltage around zero. As a result the distortion of both, capacitor voltage and a.c. input current will be minimal even at a relatively large voltage window "h". On the other hand, from Fig.4.5 it can be seen that the average output d.c.

voltage will be less (due to the presence of negative voltage pulses) as compared to the previous mode of operation (with inter-phase diodes).

The average output d.c. voltage for single phase bridge can be estimated by applying the method of "Local Average" [30]. The result for both modes of operation turned out to be the same as given by eq.(4.1).

$$V_{out}(V_{dc}) = V_c(t_o)(i_1-mC)/i_{dc} \qquad (4.1)$$

where $m=dV_c/dt$ evaluated at $t=t_o$.

In eq.4.1, when the term in the bracket changes sign then the d.c. voltage also changes sign resulting in reversal of power. This situation can only happen when the converter is operated without the inter-phase diodes.

4.3 PARAMETER CONSTRAINTS

This section presents parameter constraints. These constraints are mainly based on experimental tests.

The range of parameter values given hereafter were used during the tests for the following range of input and output voltages and currents:

A.C. input voltage: 20-90V

A.C. input current: Up to 5A

D.C. output current: Up to 14A

D.C. output voltage: Up to 150V (R load: $V_{out}=I_{dc}R$, where I_{dc} is the d.c. current and R is the load resistor).

4.3.1 A.C. Capacitance, C

The switching function of the converter relies on charging and discharging the a.c. capacitor. Large capacitors draw large a.c. currents. Furthermore, large capacitors take long time periods of charging and discharging which result into low switching frequency. Small capacitors draw minute a.c. currents. But small capacitors charge and discharge in very short time periods. There will be overshoots of the capacitor voltage beyond the two reference bounds due to delay between signal detection and switching action. In addition, small capacitors will impose high switching losses due to high switching frequency.

In order to be able to operate the converter satisfactorily, the a.c. capacitor should be chosen to suit the above mentioned conditions. In the experimental tests of this converter, the range of values of the a.c. capacitor used is between 20μF and 100μF. Large capacitors suit high current operation and vice-versa.

4.3.2 A.C. source resistance, R_s

A resistive element introduces losses which are undesirable. However resistive element have an advantage of damping the system. Since in the industrial system there is

always some resistance in any circuit, then it is logical to consider this situation in any electrical system. The resistance on the a.c. side during the tests was about 1.0Ω.

4.3.3 A.C. source inductance, L_1

This parameter is always present in a.c. circuits in the form of leakage inductance of the transformers, etc. As described in chapter II, the input parameter block in the control circuit provides power factor regulation around unity. The a.c. source inductance on the a.c. side during the test was 10mH.

4.3.4 The Proportional Control Gain, K_p

It is well known from literature in control that the control gain plays a vital role in the stability of the controlled system. In general the system becomes unstable when the control gain exceeds certain limit.

Since this documentation is the first for this system, it is worthwhile to give the range of K_p values used during the tests. These are from 1.0 to 4.0.

4.3.5 The D.C. link Inductance, L_2

The vital role of this parameter is to impose large time constant on the d.c. link so as to keep the d.c. current ripple at minimum level. The larger the value of the d.c. inductance the better the output d.c current. However, very

large d.c. inductors are very expensive. Therefore, the constraint here lies on the desired quality of the output d.c. current and cost.

Two, 100mH each, d.c. inductors were available in the laboratory. So that inductances of 50, 100 and 200mH were used.

4.4 SUMMARY

Two different modes of operation of the converter were described. It was shown that at large voltage window the inter-phase diodes introduce distortions of capacitor voltage and the a.c. source current.

Operation without inter-phase diodes eliminates the distortion of capacitor voltage and a.c. source current. More interesting, this mode of operation allow some power to be returned to the a.c. side but the average output d.c. voltage is smaller.

The parameter constraints were briefly discussed and parameter ranges used during the tests were given.

The next chapter presents the test results of the converter. The test results obtained before implementation of the "Modified" comparison and logic circuits will confirm the arguments presented in the last part of chapter II.

CHAPTER V

EXPERIMENTAL TEST RESULTS OF DELTA MODULATED CONVERTER

Chapter II gives a detailed description of the control strategy used. In addition, the method of measuring three phase capacitor voltages was described.

Chapter III described the basic circuit elements of the electronic switches used in this converter. The electronic switches consist of power transistors, snubber circuits and base drive circuits. Detailed design of the base drive circuits is given in [15,16,33]. Chapter IV described two possible operating modes of the converter together with the range of parameter values used during the tests.

This chapter presents the test results of the converter. All test results were obtained with a resistor load on the d.c. link. Test results obtained with m1 and m2 signals (with original VC and BDL circuits) are presented. These results illustrate the need of changing the comparison and logic circuits to their "Modified" versions as discussed in chapter II.

With the MVC and MBDL circuits, the results for the two operating modes described in chapter IV are presented. The quality of the waveforms verify the PWM strategy proposed and the control circuitry used.

5.1 ORIGINAL VC AND BDL CIRCUITS

With the original VC and BDL circuits (presence of m1 and m2 signals), there is a conduction overlap period of the two transistor groups around zero crossing of the capacitor voltage (see Fig.2.12). This period is equal to the voltage window. This situation causes distortion of the capacitor voltage as well as the a.c. source current.

Figure 5.1 shows the waveforms of (from top to bottom) d.c. current, capacitor voltage, a.c. source voltage and a.c. source current. The waveforms illustrate a near sinusoidal a.c. current and unity power factor.

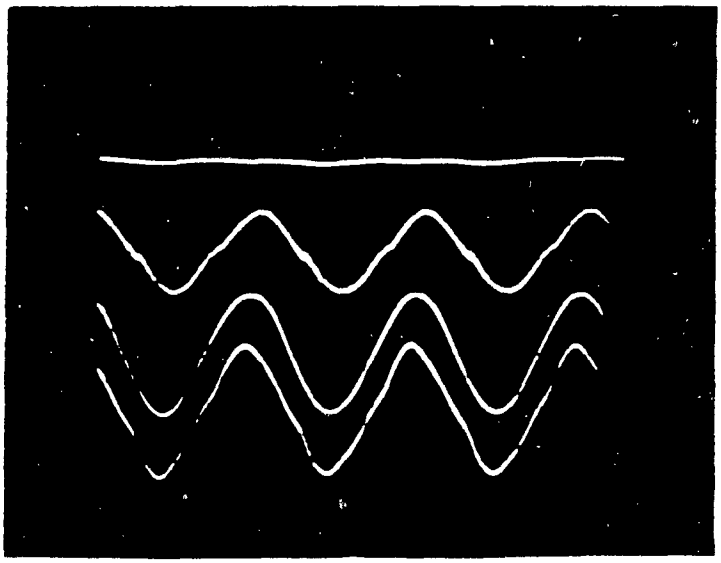


Fig.5.1 Test results with original VC and BDL circuits.

Figure 5.2 shows the three phase capacitor voltages when the converter is in operation. These waveforms verify

the distortion of the capacitor voltage discussed in the previous chapters. The distortion is caused by the large overlap conduction period of the two transistor groups (see Fig.2.12). Awareness of the voltage distortion led to the re-design the voltage comparison and base drive logic circuits. All other tests were done with the MVC and MBDL circuits.

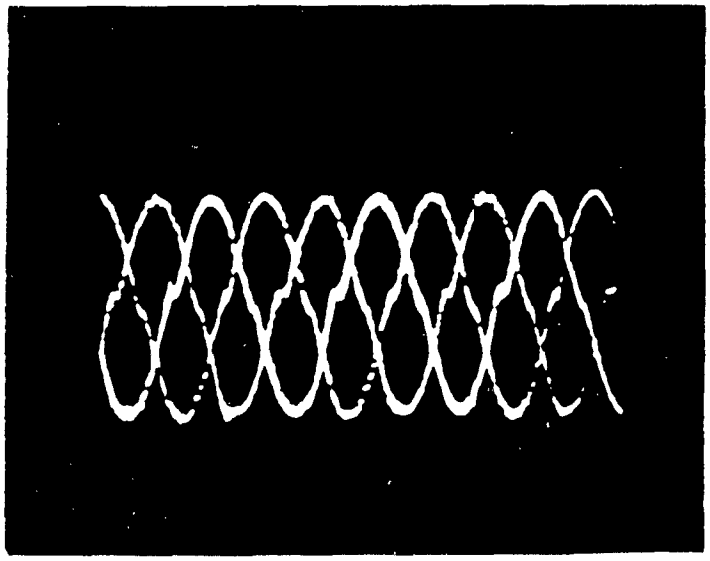


Fig.5.2 3-phase capacitor voltages showing distortion.

5.2 MODIFIED VC AND BDL CIRCUITS (MVC AND MBDL)

The test results presented in section 5.1 have shown distortion caused by overlap conduction of the two transistor groups of the H-bridge. This section presents test results obtained with MVC and MBDL circuits. The test results for the two operating modes explained in chapter IV are presented.

5.2.1 Operation with inter-phase diodes

When the voltage window is large, the waveforms obtained in this mode of operation are similar to those shown in section 5.1. With small voltage window the distortion of capacitor voltage can be suppressed. On the other hand this mode of operation provides higher d.c. output voltage as compared to the other mode of operation (see Fig.4.1 and 4.5).

Fig.5.3 shows the waveforms of (from top to bottom) d.c. current, capacitor voltage, a.c. source voltage and a.c. source current. From Fig.5.3 it can be seen that the a.c. source current is near sinusoidal and in phase with the respective phase voltage.

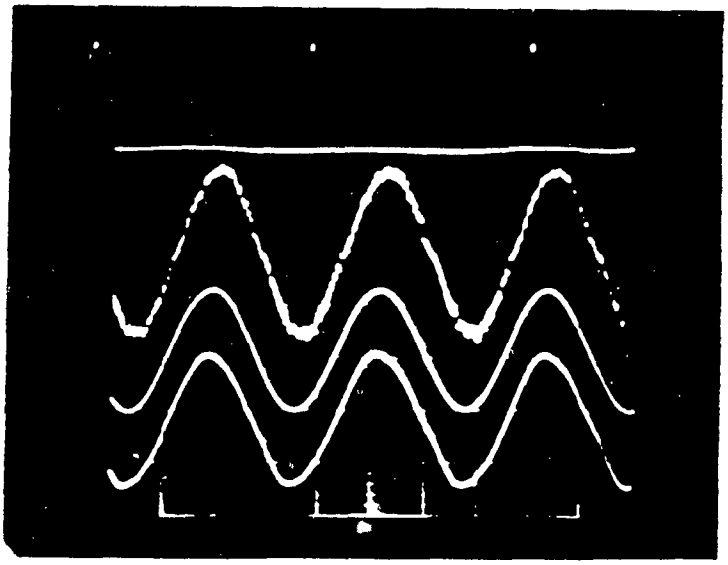


Fig.5.3 Test results with (MVC) and (MBDL) circuits.

Fig.5.4 shows the a.c. source current and its Fourier Transform. From the Fourier Transform of the a.c. source current it can be seen that the harmonic content is minimum.

Fig.5.5 shows three phase a.c. source currents. Fig.5.6 shows three phase capacitor voltages as detected by Opto-coupler capacitor voltage measuring circuit. Fig.5.7 shows capacitor voltage waveform with large voltage window. Fig.5.8 shows the expanded time scale of Fig.5.7 around zero crossing. The inter-phase diode cause dead zone of the capacitor voltage around zero crossing.

Fig.5.9 illustrates the capability of the converter to operate at leading power factor: (from top to bottom) d.c. current, capacitor voltage, a.c. source voltage and current. Fig.5.10 shows the same waveforms as in Fig.5.9 but illustrating operation at lagging power factor.

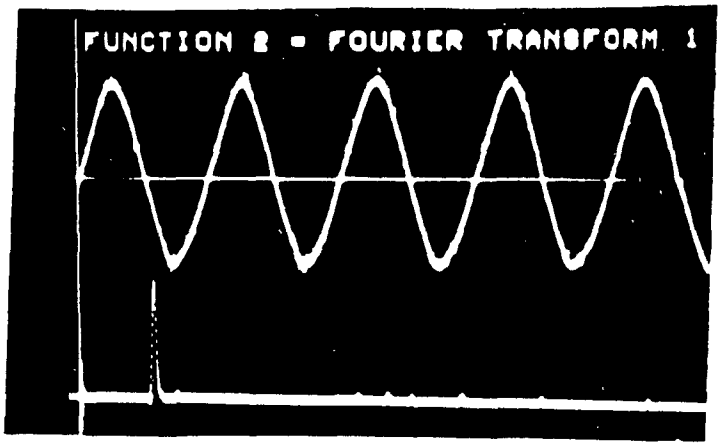


Fig.5.4 A.C. source current with its Fourier Transform.

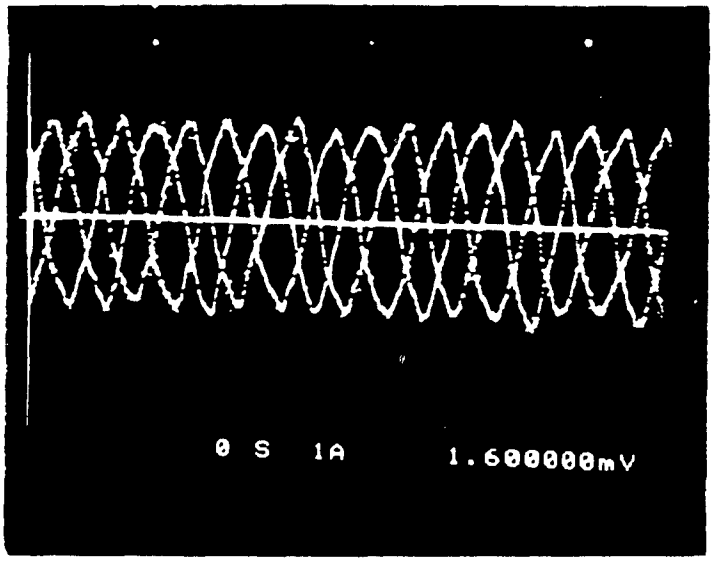


Fig.5.5 Three phase a.c. source currents.

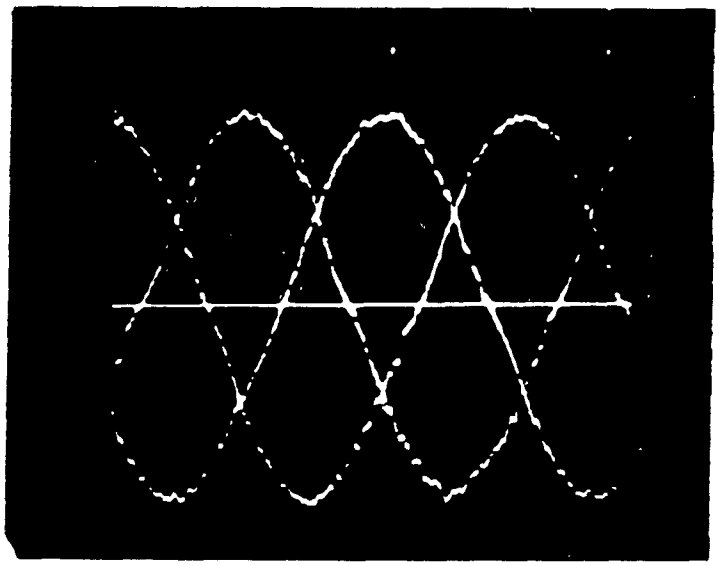


Fig.5.6 Three phase capacitor voltages.

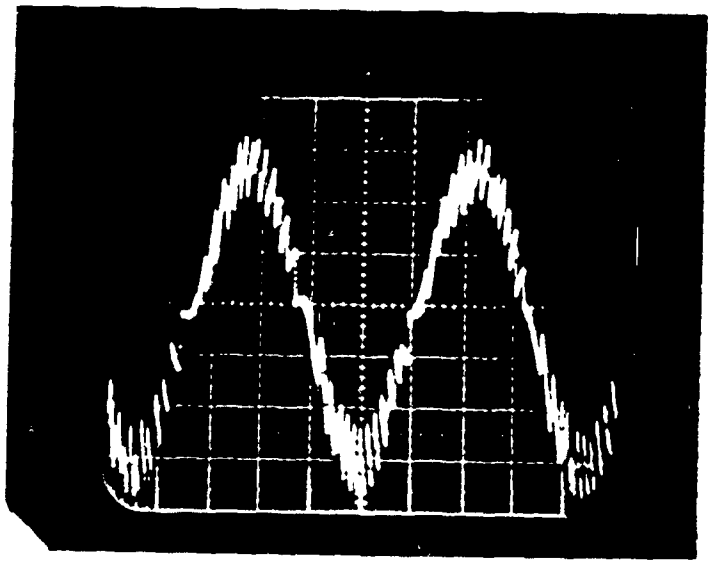


Fig.5.7 Capacitor voltage with large voltage window.

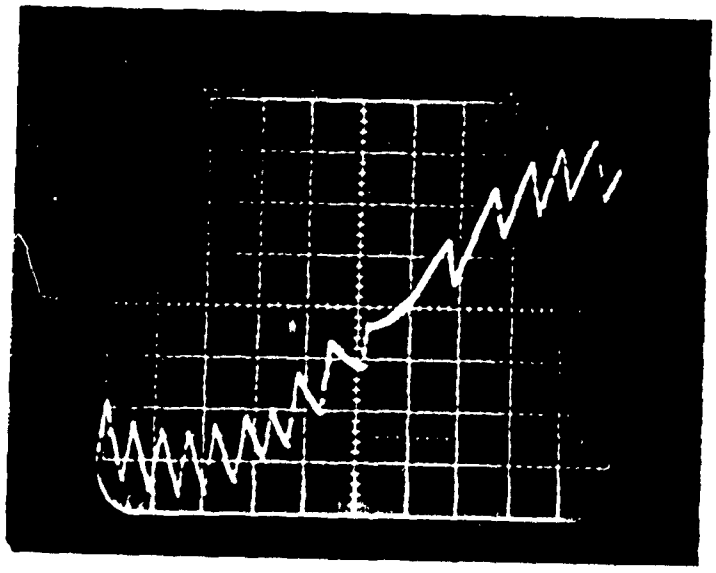


Fig.5.8 Expanded time scale of Fig.5.7.

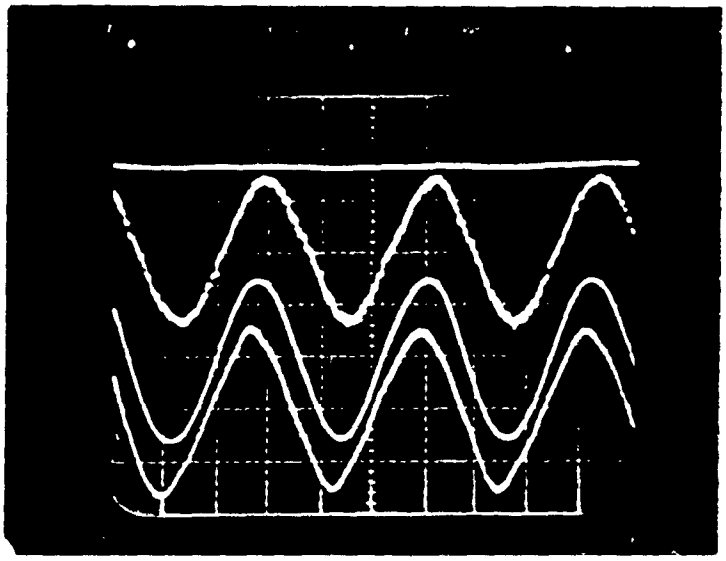


Fig.5.9 Marginal leading power factor.

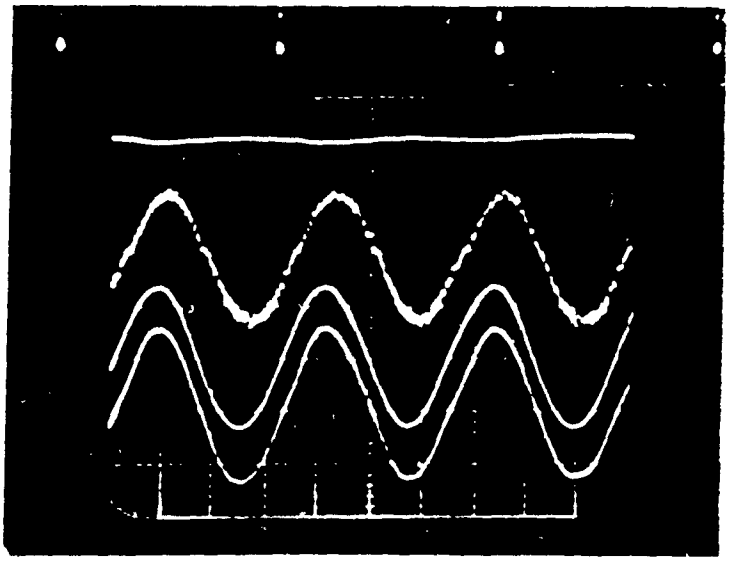


Fig.5.10 Marginal lagging power factor.

Fig.5.11 shows the Current Regulation curve under proportion feedback control. The current reference has been set at I_{REF} = 12Amps. The feedback proportionality constants have been K_p=1, K_p=2 and K_p=3. As expected, the regulation is better when the feedback gain is higher.

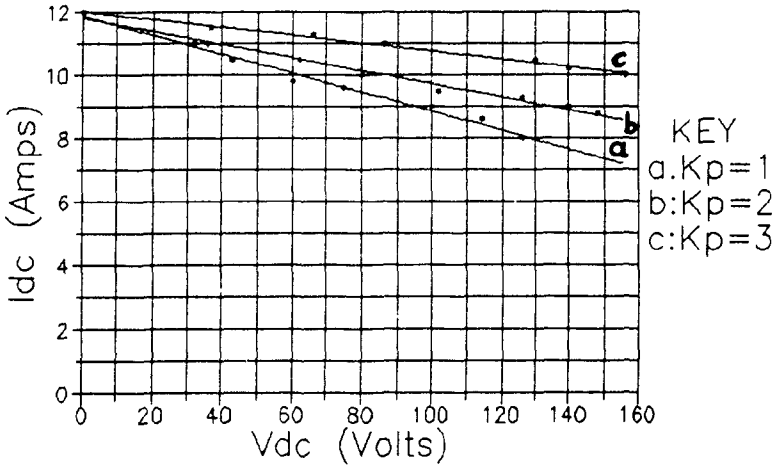


Fig.5.11 DC Current Regulation Curve.

5.2.2 Operation without inter-phase diodes

Proper operation of this mode requires perfect operation of the entire system. Since the three phases are connected in series, a single malfunction of any part in the system will lead to over-voltage due to the DC inductive current. Otherwise, this mode of operation introduces no distortion other than switching ripple if the current drawn from the a.c. source is high enough to suppress the power frequency capacitor current.

Figure 5.12 shows the waveforms of (from top to bottom) d.c. current, capacitor voltage, a.c. source voltage and a.c. source current. It can be seen that the a.c. source current is distorted and leading the voltage by about 80 degrees. This is because this mode of operation could only be conducted at very low currents. As a result the a.c. current was mainly capacitive. In order to nullify the effect of power frequency capacitive current, the d.c. current should be large. There is a limit of minimum value of d.c. current at which the control circuitry is superior to effect variations of power factor etc. Presence of high instantaneous negative peaks of d.c. voltage due to $L_2 di_4/dt$ during voltage raise time periods hindered high current operation. Protection against $L_2 di_4/dt$ is needed in order to be able to conduct this mode of operation successfully.

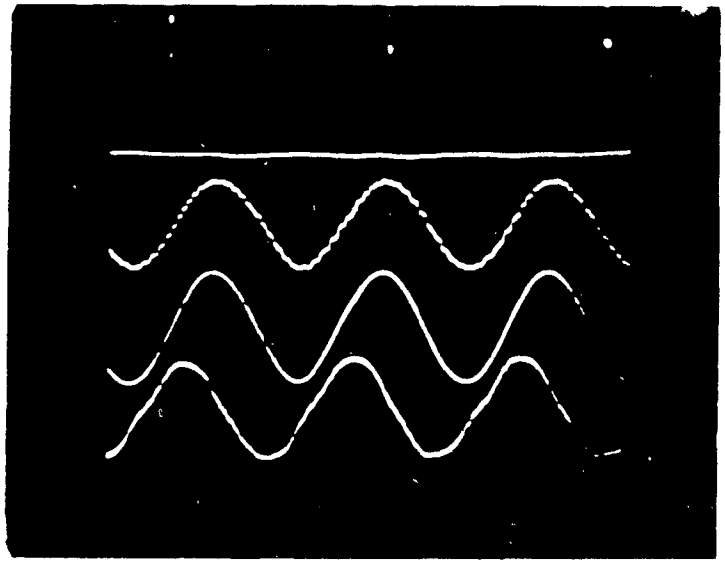


Fig.5.12 Test results without inter-phase diodes.

Fig.5.13 shows capacitor voltage waveform with large voltage window. The waveform shows no dead zone around zero which confirms the description given in chapter IV (see Fig.4.5).

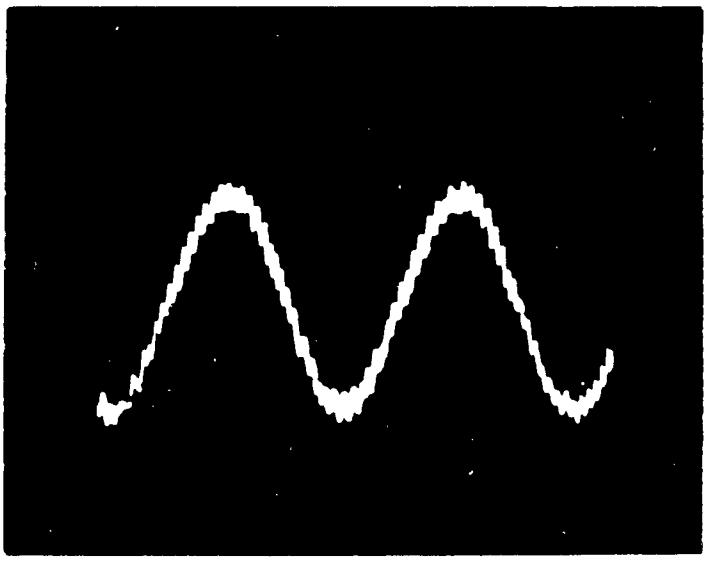


Fig.5.13 Capacitor voltage with large voltage window.

5.3 SUMMARY

In this chapter, the experimental test results for the converter were presented. The test results in the presence of m1 and m2 signals were presented and proved the need of modifying the VC and BDL circuits as explained in the last part of chapter II.

Test results obtained with the (MVC) and (MBDL) circuits were presented. The results proved the ability of

the converter to operate at unity power factor and even leading power factor with closed regulation of the DC current.

CHAPTER VI

CONCLUSIONS

6.1 SUMMARY

The aims of this research work leading to the thesis has been to construct and to test a three phase delta modulated buck type PWM converter. Such a converter is a dual of the existing current hysteresis boost type PWM converter. The dual nature led to the implementation of the engineering hardware which aimed at verifying this concept rather than embarking on detailed design. The converter was constructed and tested under steady state conditions.

This thesis contains documentation of the early stages of practical realization of this converter topology. Further evaluation of the performance characteristics of the system requires a broad range of experimental tests in hand with theoretical analysis. This will lead to proper dimensioning of the components described in Chapter IV for a desired rating of the converter. Due to the financial time limit set by German Academic Exchange Service (DAAD) and University of Dar es Salaam, this research covers the construction and test of the converter only.

6.2 CONCLUSIONS

From the preliminary test results, the following conclusions can be drawn concerning the converter:

(1) The converter draws near sinusoidal a.c. currents with minimum harmonic content.

(2) The input power factor can be marginally regulated around unity.

(3) Presence of a.c. capacitor and indirect switching of the a.c. current through the capacitor voltage, makes the a.c. current even cleaner of switching ripples.

(4) The DC current is closely regulated.

(5) High quality a.c. currents can be achieved for switching frequencies as low as 2kHz with proper adjustment of the voltage window and the a.c. capacitor. This fact is illustrated in Fig.6.1, showing a.c. source current (upper), capacitor voltage within the voltage window (lower). Low switching frequency means low switching losses resulting in high system efficiency.

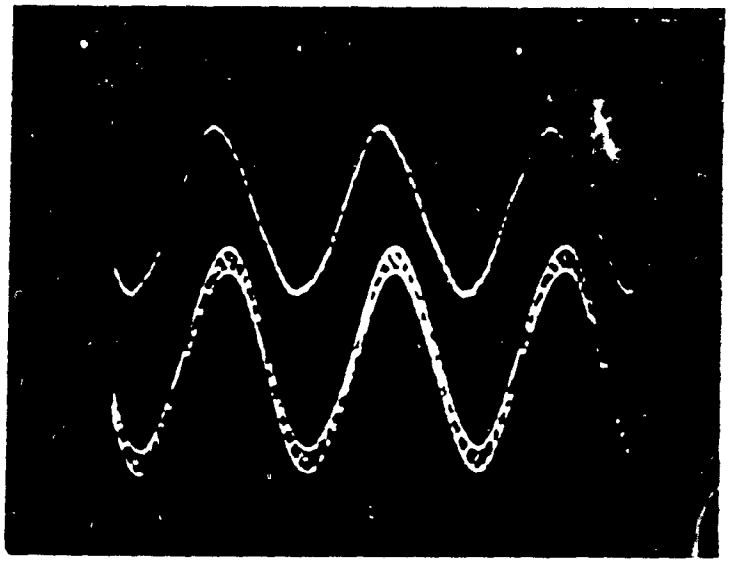


Fig.6.1 Waveforms of A.C. source current and capacitor voltage within the voltage window at low switching frequency.

6.3 DISCUSSION

This converter topology has two disadvantages:

(i) The requirement of floating transformer secondaries.

(ii) The need of twice the number of electronic switches as compared to the existing three phase bridge PWM converters.

These two disadvantages lead one to conclude that this converter topology is more expensive than the existing current source PWM converters. But the judgement should wait until comparative performance evaluations become available.

The converter was made to function as delta modulated PWM buck type converter. This was achieved by controlling the capacitor voltage using the control circuitry explained in chapter II. The control involved four stages: voltage template derivation, capacitor voltage measurement, voltage comparison and base drive logic circuitry. The test results showed that the circuits worked satisfactorily.

However, the opto-coupler capacitor voltage measurement circuitry could be improved. At the beginning of the project it was anticipated that the capacitor voltage measurement would be accomplished by a hall effect voltage sensor. Later, it was found that the type of industrial sensor chosen had small bandwidth compared to the anticipated

switching frequency. The opto-coupler option was therefore chosen. The need of circuit isolation and high bandwidth detection necessitated the use of opto-coupler voltage measurement circuitry. The problem is to obtain three matched opto-couplers which have the same gain for the three phases of the converter. Moreover there is the problem of linearity and drift of the opto-coupler gain with respect to temperature variation.

On the other hand, the bandwidth of the opto-coupler circuitry is limited by the bandwidth of the amplifiers used at the input and output. True detection of the capacitor voltage was therefore a problem. The details for the choice of amplifiers in the opto-coupler circuitry are given in chapter II.

6.4 SUGGESTIONS FOR FURTHER WORK

From the test results, the following suggestions can be made:

(i) In order to explore further the performance characteristics of the converter, high quality voltage transducers should be used.

(ii) The d.c. load resistor should be replaced by a more ideal current source d.c. load which provides large time constant.

(iii) Operation of the converter without inter-phase diodes requires further consideration. In this thesis, the

assurance of the DC current path have been done across the single phase bridges only which appeared to be insufficient especially at high current operation. The correct way is to ensure the DC current path through all the three single phase bridges all the time. Furthermore protection against $L_2 di_4/dt$ is needed.

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APPENDICES

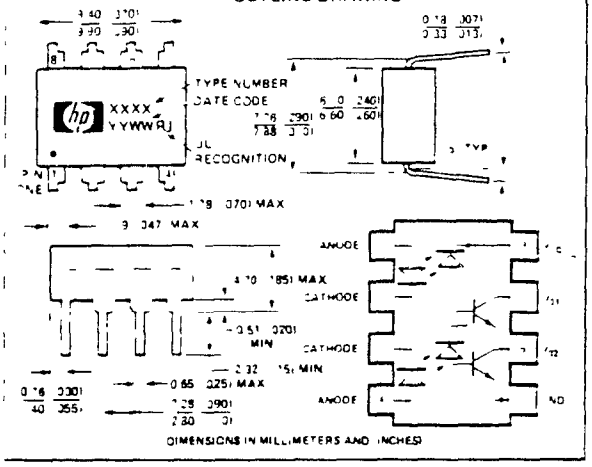
APPENDIX A: HCPL2530 DUAL HIGH SPEED OPTO-COUPLER

HEWLETT PACKARD

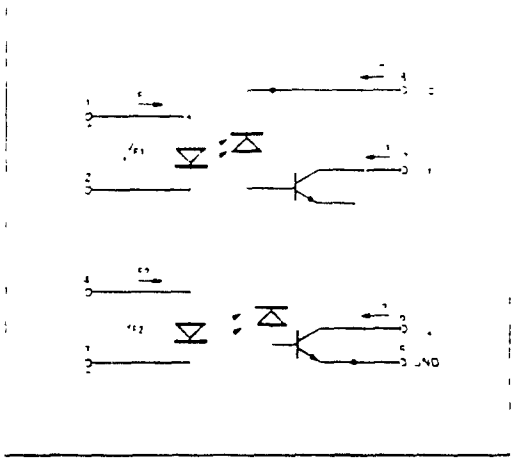
DUAL HIGH SPEED OPTOCOUPLER

HCPL-2530
HCPL-2531

OUTLINE DRAWING



SCHEMATIC



Features

- **HIGH SPEED: 1 Mbit/s**
- **TTL COMPATIBLE**
- **HIGH COMMON MODE TRANSIENT IMMUNITY: >1000V/μs**
- **HIGH DENSITY PACKAGING**
- **DIELECTRIC WITHSTAND TESTED AT 2500 Vac FOR A WORKING VOLTAGE OF 220 Vac**
- **3 MHz BANDWIDTH**
- **OPEN COLLECTOR OUTPUTS**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES, INC. (FILE NO E55361)**

Description

The HCPL-2530/31 dual couplers contain a pair of light emitting diodes and integrated photon detectors with electrical insulation between input and output. Separate connection for the photodiode bias and output transistor collectors improve the speed up to a hundred times that of a conventional phototransistor coupler by reducing the base-collector capacitance.

The HCPL-2530 is suitable for use in TTL, CMOS, TTL, LSTTL or wide bandwidth analog applications. Current transfer ratio, CTR, for the -2530 is 7% minimum at I_F = 16 mA.

The HCPL-2531 is suitable for high speed TTL/TTL applications. A standard 16 mA TTL sink current through the input LED will provide enough output current for 1 TTL load and a 5.6 kΩ pull up resistor. CTR of the -2531 is 19% minimum at I_F = 16 mA.

Applications

- **Line Receivers** – High common mode transient immunity (>1000V/μs) and low input output capacitance (0.6pF).
- **High Speed Logic Ground Isolation** – TTL/TTL, TTL/LTTL, TTL/CMOS, TTL/LSTTL.
- **Replace Pulse Transformers** – Save board space and weight.
- **Analog Signal Ground Isolation** – Integrated photon detector provides improved linearity over phototransistor type.
- **Polarity Sensing.**
- **Isolated Analog Amplifier** – Dual channel packaging enhances thermal tracking.

OPTOCOUPLERS

Absolute Maximum Ratings

Storage Temperature	-55°C to +125°C
Operating Temperature	-55°C to +100°C
Lead Solder Temperature	260°C for 10s (1.6mm below seating plane)
Average Input Current – I_F (each channel)	25mA[1]
Peak Input Current – I_F (each channel) (50% duty cycle, 1 ms pulse width)	50mA[2]
Peak Transient Input Current – I_F (each channel) (≤1μs pulse width, 300pps)	1.0A
Reverse Input Voltage – V_R (each channel)	5V
Input Power Dissipation (each channel)	45mW[3]
Average Output Current – I_O (each channel)	8mA
Peak Output Current – I_O (each channel)	16mA
Supply and Output Voltage – V_{CC} (Pin 8-5) V_O (Pin 7-6-5)	-0.5V to 15V
Output Power Dissipation (each channel)	35mW[4]

See notes, following page

Electrical Specifications

Over recommended temperature (T_A = 0°C to 70°C unless otherwise specified

Parameter	Sym	Device HCPL	Min	Typ**	Max	Units	Test Conditions	Fig	Note
Current Transfer Ratio	CTR	2530	7	18		%	I_F = 16mA, V_O = 0.5V, V_{CC} = 4.5V, T_A = 25°C	1,2	5,6
		2531	19	24		%			
		2530	5	13		%	I_F = 16mA, V_O = 0.5V, V_{CC} = 4.5V		
		2531	15	21		%			
Logic Low Output Voltage	V_{OL}	2530		0.1	0.5	V	I_F = 16mA, I_O = 1.1mA, V_{CC} = 4.5V, T_A = 25°C		5
		2531		0.1	0.5	V	I_F = 16mA, I_O = 2.4mA, V_{CC} = 4.5V, T_A = 25°C		
Logic High Output Current	I_{OH}			3	500	nA	T_A = 25°C, I_{F1} = I_{F2} = 0, V_{O1} = V_{O2} = V_{CC} = 5.5V	6	5
					50	µA	I_{F1} = I_{F2} = 0, V_{O1} = V_{O2} = V_{CC} = 15V		5
Logic Low Supply Current	I_{CCL}			80		µA	I_{F1} = I_{F2} = 16mA, V_{O1} = V_{O2} = Open, V_{CC} = 15V		
Logic High Supply Current	I_{CCH}			0.05	4	µA	I_{F1} = I_{F2} = 0mA, V_{O1} = V_{O2} = Open, V_{CC} = 15V		
Input Forward Voltage	V_F			1.5	1.7	V	I_F = 16mA, T_A = 25°C	3	5
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.6		mV/°C	I_F = 16mA		5
Input Reverse Breakdown Voltage	V_R		5			V	I_F = 10µA, T_A = 25°C		5
Input Capacitance	C_{IN}			60		pF	f = 1MHz, V_F = 0		5
Input - Output Insulation Leakage Current	I_{I-O}				1.0	µA	45% Relative Humidity, t = 5s, V_{I-O} = 3000Vdc, T_A = 25°C		7,13
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500Vdc		7
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1MHz		7
Input-Input Insulation Leakage Current	I_{I-I}			0.005		µA	45% Relative Humidity, t = 5s, V_{I-I} = 500Vdc		8
Resistance (Input-Input)	R_{I-I}			10^{11}		Ω	V_{I-I} = 500Vdc		8
Capacitance (Input-Input)	C_{I-I}			0.25		pF	f = 1MHz		8

**All typicals at 25°C

Switching Specifications at T_A = 25°C V_{CC} = 5V, I_F = 16mA, unless otherwise specified

Parameter	Sym	Device HCPL-	Min	Typ	Max	Units	Test Conditions	Fig	Note
Propagation Delay Time To Logic Low at Output	t_{PHL}	2530		0.3	1.5	µs	R_L = 4.1kΩ	5,9	10,11
		2531		0.2	0.8	µs	R_L = 1.9kΩ		
Propagation Delay Time to Logic High at Output	t_{PLH}	2530		0.4	1.5	µs	R_L = 4.1kΩ	5,9	10,11
		2531		0.3	0.8	µs	R_L = 1.9kΩ		
Common Mode Transient Immunity at Logic High Level Output	CM_H	2530		1000		V/µs	I_F = 0mA, R_L = 4.1kΩ, V_{CM} = $10V_{p-p}$	10	9,10,11
		2531		1000		V/µs	I_F = 0mA, R_L = 1.9kΩ, V_{CM} = $10V_{p-p}$		
Common Mode Transient Immunity at Logic Low Level Output	CM_L	2530		-1000		V/µs	V_{CM} = $10V_{p-p}$, R_L = 4.1kΩ	10	9,10,11
		2531		-1000		V/µs	V_{CM} = $10V_{p-p}$, R_L = 1.9kΩ		
Bandwidth	BW			3		MHz	R_L = 100Ω	8	12

NOTES

1. Derate linearly above 70°C free-air temperature at a rate of 0.8mA/°C.
2. Derate linearly above 70°C free-air temperature at a rate of 1.6mW/°C.
3. Derate linearly above 70°C free-air temperature at a rate of 2.0mW/°C.
4. Each channel.
5. CURRENT TRANSFER RATIO (CTR) is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
6. Device considered a two terminal device: Pins 1, 2, 3 and 4 shorted together and Pins 5, 6, 7 and 8 shorted together.
7. Measured between pins 1 and 2 shorted together, and pin 3, 4 and 5 shorted together.
8. Common mode transient immunity in Logic High level is the maximum tolerable positive dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0V). Common mode transient immunity in Logic Low level is the maximum tolerable negative dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8V).
9. The 1.9kΩ load represents 1 TTL unit load of 1.6mA and the 5.6kΩ pull-up resistor.
10. The 4.1kΩ load represents 1 TTL unit load of 1.6mA and the 2.4kΩ pull-up resistor.
11. The frequency at which the ac output voltage is 3dB below the low frequency asymptote.
12. See Figure 8 for test circuit. Specification is for device with external pull-up resistor.
13. Device is considered a two terminal device: Pins 1, 2, 3 and 4 are shorted together and Pins 5, 6, 7 and 8 are shorted together.

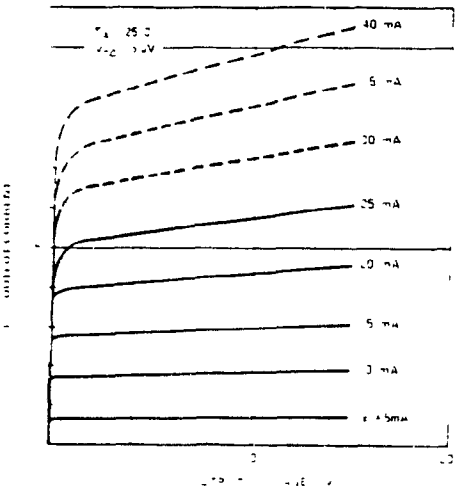


Figure 1. DC and Pulsed Transfer Characteristics

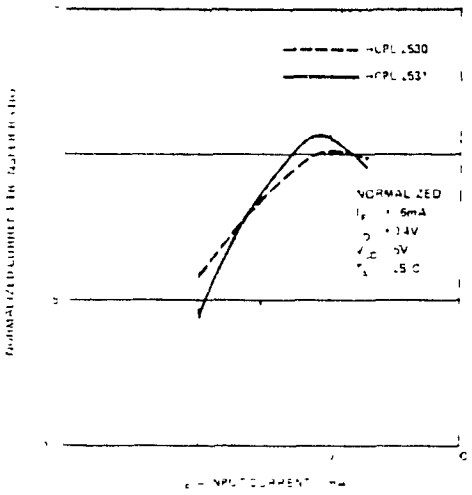


Figure 2. Current Transfer Ratio vs. Input Current

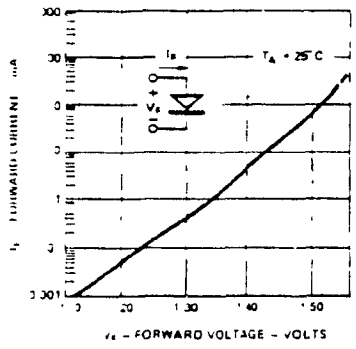


Figure 3. Input Current vs. Forward Voltage.

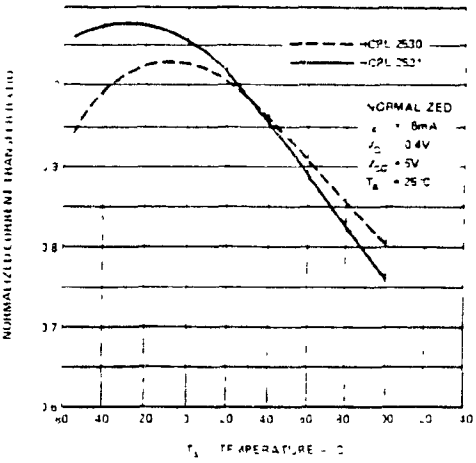


Figure 4. Current Transfer Ratio vs. Temperature

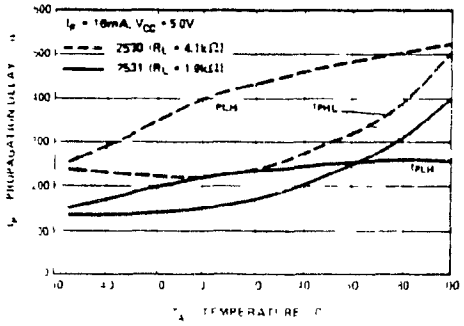


Figure 5. Propagation Delay vs. Temperature

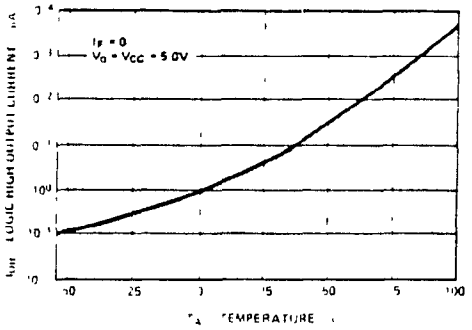


Figure 6. Logic High Output Current vs. Temperature

OPTOCOUPLERS

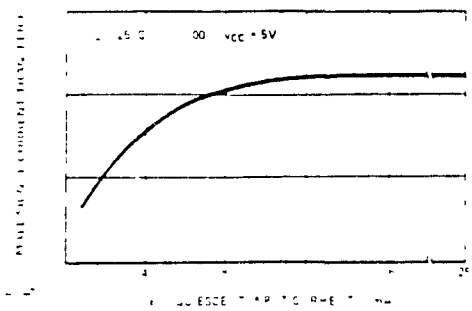


Figure 7 Small Signal Current Transfer Ratio vs Quiescent Input Current

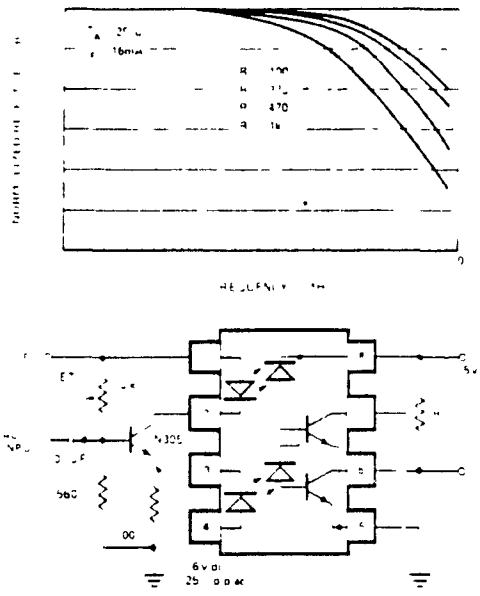


Figure 8 Frequency Response

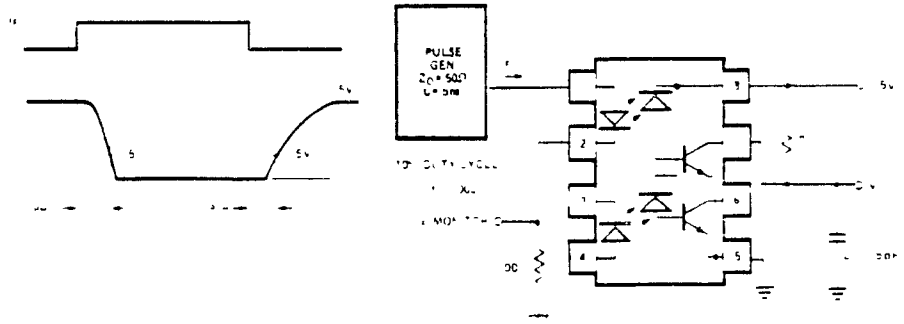


Figure 9 Switching Test Circuit

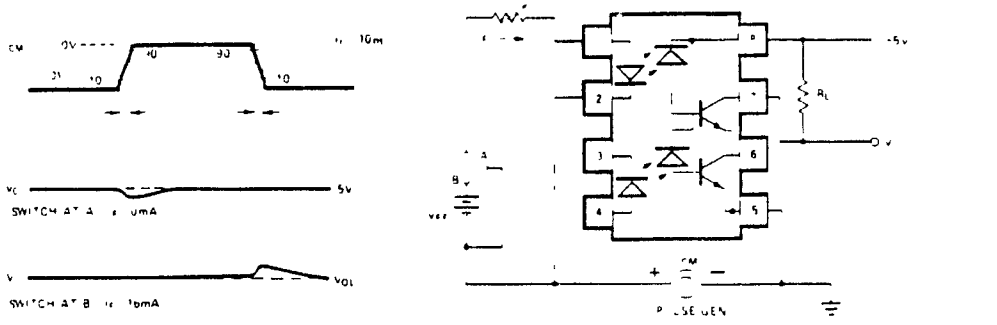


Figure 10 Test Circuit for Transient Immunity and Typical Waveforms

APPENDIX B: POWER TRANSISTOR DATA SHEET

MJ10015
MJ10016

1.3

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS
WITH BASE EMITTER SPEEDUP DIODE

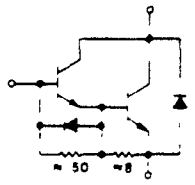
The MJ10015 and MJ10016 Darlington transistors are designed for high voltage, high speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as

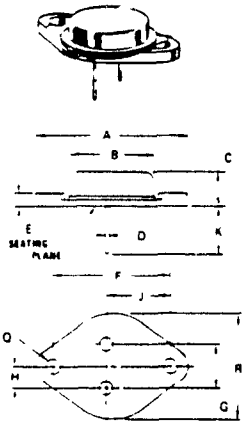
- Switching Regulators
- Motor Controls
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times
  - 1.0 µs (max) Inductive Crossover Time – 20 Amps
  - 2.5 µs (max) Inductive Storage Time – 20 Amps
- Operating Temperature Range -65 to +200°C
- Performance Specified for
  - Reversed Biased SOA with Inductive Loads
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents

50 AMPERE

NPN SILICON POWER DARLINGTON TRANSISTORS

400 and 500 VOLTS
250 WATTS





STYLE 1
PIN 1 BASE
2 EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01
MODIFIED TO 3

MAXIMUM RATINGS

Rating	Symbol	MJ10015	MJ10016	Unit
Collector Emitter Voltage	$V_{CEO(sus)}$	400	500	Vdc
Collector Emitter Voltage	V_{CEV}	600	700	Vdc
Emitter Base Voltage	V_{EB}	8.0		Vdc
Collector Current – Continuous – Peak (1)	I_C I_{CM}	50 75		Adc
Base Current – Continous – Peak (1)	I_B I_{BM}	10 15		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	250 143 1.43		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%

1.3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)						
Collector Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0, V_{clamp} = Rated V_{CEO})	MJ10015 MJ10016	$V_{CEO(sus)}$	 400 500	 – –	 – –	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)		I_{CEV}	–	–	0.25	mAdc
Emitter Cutoff Current (V_{EB} = 2.0 Vdc, I_C = 0)		I_{EBO}	–	–	350	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with Base Forward Biased		$I_{s/b}$	See Figure 7			
Clamped Inductive SOA with Base Reverse Biased		RBSOA	See Figure 8			
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 20 Adc, V_{CE} = 5.0 Vdc) (I_C = 40 Adc, V_{CE} = 5.0 Vdc)		h_{FE}	 25 10	 – –	 – –	–
Collector Emitter Saturation Voltage (I_C = 20 Adc, I_B = 1.0 Adc) (I_C = 50 Adc, I_B = 10 Adc)		$V_{CE(sat)}$	 – –	 – –	 2.2 5.0	Vdc
Base-Emitter Saturation Voltage (I_C = 20 Adc, I_B = 1.0 Adc)		$V_{BE(sat)}$	–	–	2.75	Vdc
Diode Forward Voltage (2) (I_F = 20 Adc)		V_f	–	2.5	5.0	Vdc
DYNAMIC CHARACTERISTIC						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)		C_{ob}	–	–	750	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 250 Vdc, I_C = 20 A, I_{B1} = 1.0 Adc, $V_{BE(off)}$ = 5 Vdc, t_p = 25 μs, Duty Cycle ≤ 2%)	t_d	–	0.14	0.3	μs
Rise Time		t_r	–	0.3	1.0	μs
Storage Time		t_s	–	0.8	2.5	μs
Fall Time		t_f	–	0.3	1.0	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_C = 20 A(pk), V_{clamp} = 250 V, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5.0 Vdc)	t_{sv}	–	1.0	2.5	μs
Crossover Time		t_c	–	0.36	1.0	μs

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

(2) The internal Collector to Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

1.3

TYPICAL CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

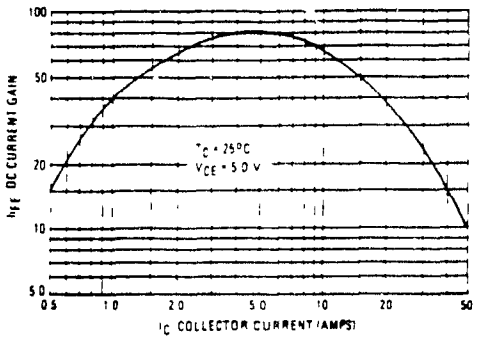


FIGURE 2 – COLLECTOR EMITTER SATURATION VOLTAGE

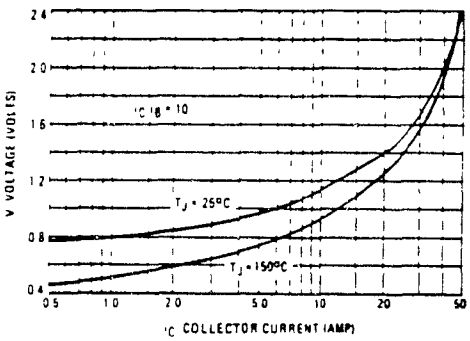


FIGURE 3 – BASE EMITTER SATURATION VOLTAGE

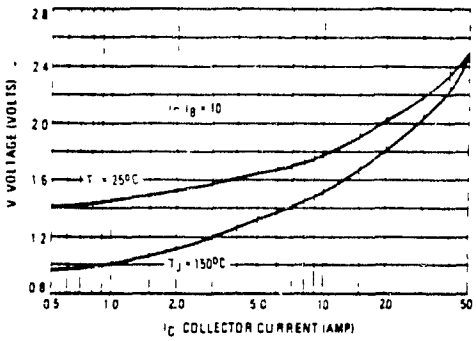


FIGURE 4 – COLLECTOR CUTOFF REGION

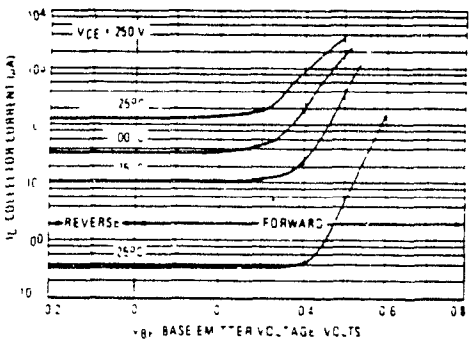


FIGURE 5 – OUTPUT CAPACITANCE

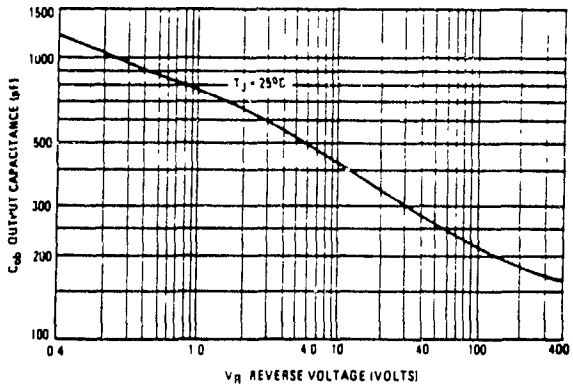
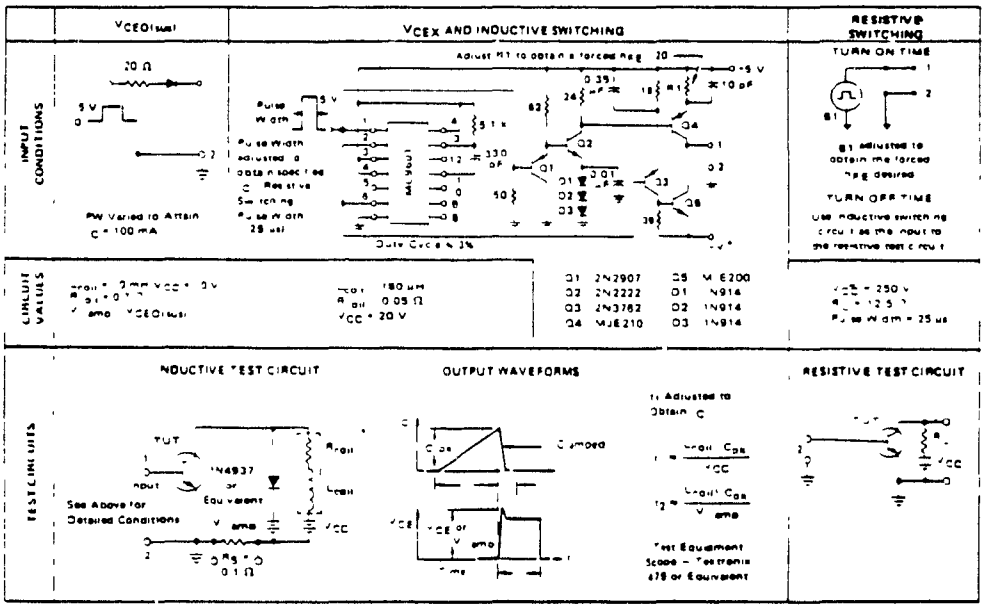
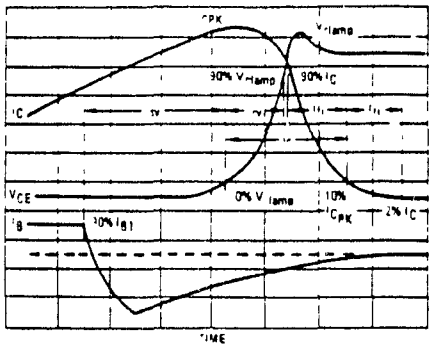


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE



*Adjust -V such that $V_{BE(off)}$ = 5 V except as required for RB SOA (Figure 8)

FIGURE 8 – INDUCTIVE SWITCHING MEASUREMENTS



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore separate measurements must be made on each waveform to determine the total switching time. For this reason the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time 10-90% V_{clamp}
t_{fi} = Current Fall Time 90-10% I_C
t_{ti} = Current Tail, 10-2% I_C
t_c = Crossover Time 10% V_{clamp} to 10% I_C

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN 222

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general $t_{rv} + t_{fi} \cong t_c$. However at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified and has become a benchmark for designers. However for designers of high frequency converter circuits, the user oriented specifications which make this a 'SWITCHMODE' transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed.

1.3

The Safe Operating Area figures shown in Figures 7 and 8 are specified ratings for these devices under the test conditions shown

FIGURE 7 – FORWARD BIAS SAFE OPERATING AREA

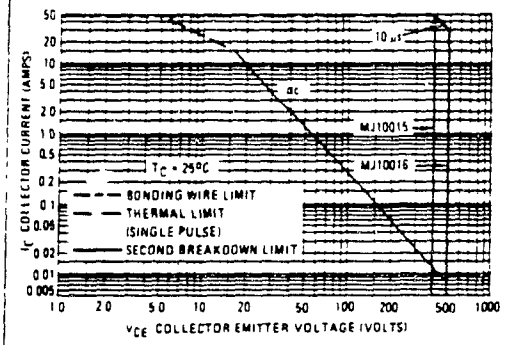
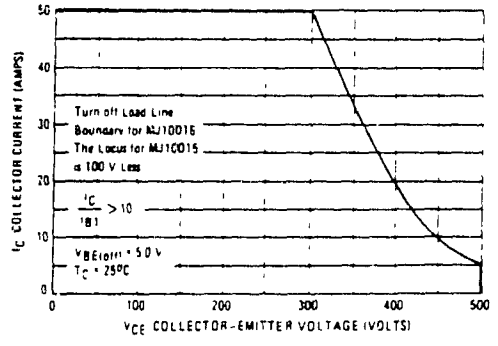


FIGURE 8 – REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor average junction temperature and second breakdown Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation i e the transistor must not be subjected to greater dissipation than the curves indicate

The data of Figure 7 is based on T_C = 25°C $T_{J(pk)}$ is variable depending on power level Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$ Second breakdown limitations do not derate the same as thermal limitations Allowable current at the voltages shown on Figure 7 may be found at any case temperature by using the appropriate curve on Figure 9

REVERSE BIAS

For inductive loads high voltage and high current must be sustained simultaneously during turn off in most cases with the base to emitter junction reverse biased Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current This can be accomplished by several means such as active clamping RC snubbing load line shaping etc The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage current condition allowable during reverse biased turn off This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode Figure 8 gives the complete RBSOA characteristics

FIGURE 9 – POWER DERATING

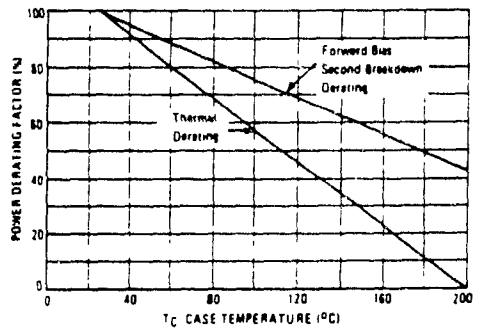
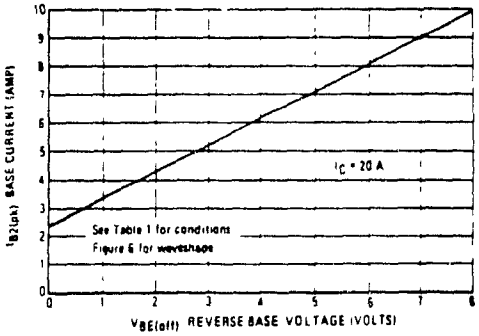


FIGURE 10 – TYPICAL REVERSE BASE CURRENT versus $V_{BE(off)}$ WITH NO EXTERNAL BASE RESISTANCE



APPENDIX C: PHYSICAL CONSTRUCTION OF THE CONVERTER

The circuits for voltage template derivation, d.c. current feedback and capacitor voltage measurement were implemented on the breadboards. This was done in order to give room for easy and quick circuit alternation.

Fig.C.1 shows the photograph of the voltage template derivation circuit including the circuit for input parameter derivation. Fig.C.2 shows the photograph of the d.c. current feedback circuit excluding the sensor which is mounted on the converter carriage. Fig.C.3 shows the photograph of the capacitor voltage measurement circuit excluding the measurement resistors.

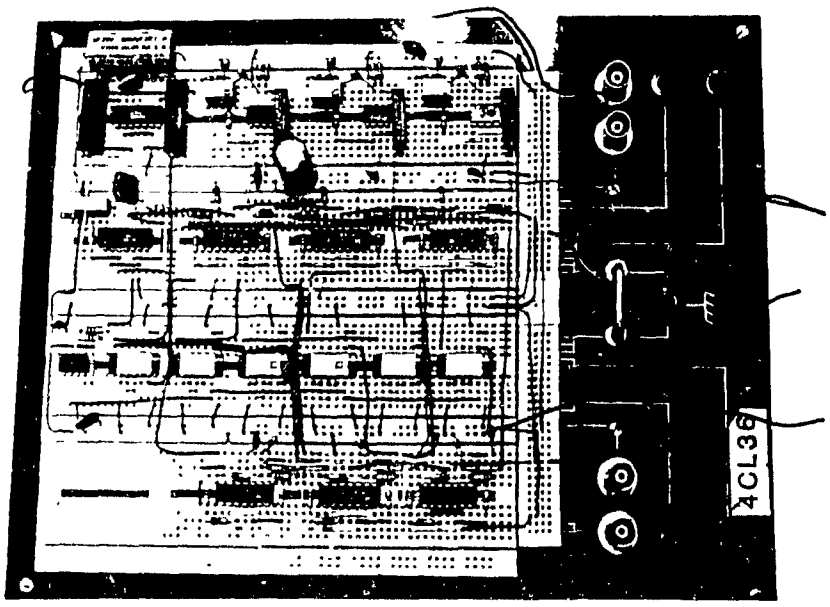


Fig.C.1 Three Phase Voltage Template Derivation Circuit (VTD).

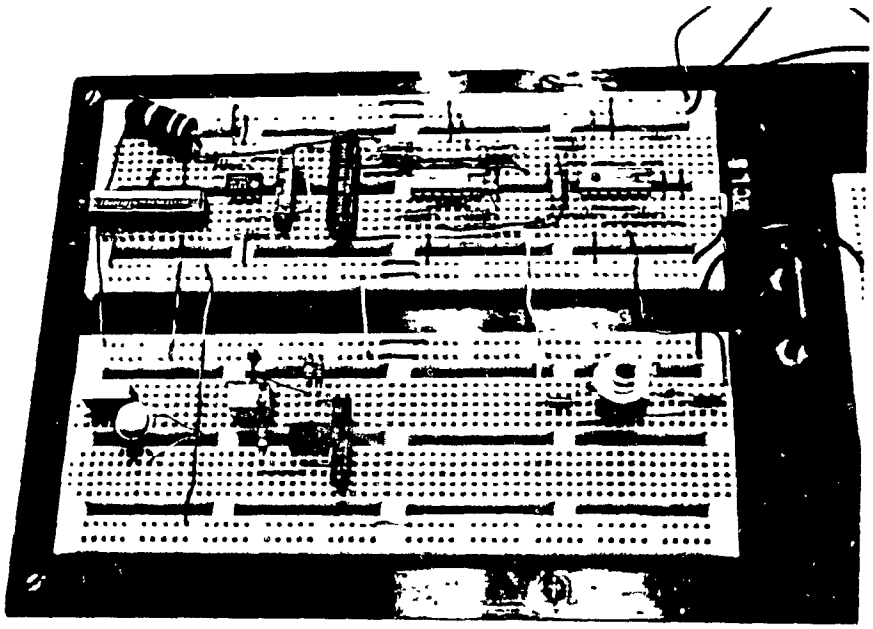


Fig.C.2 D.C. Current Feedback Circuit.

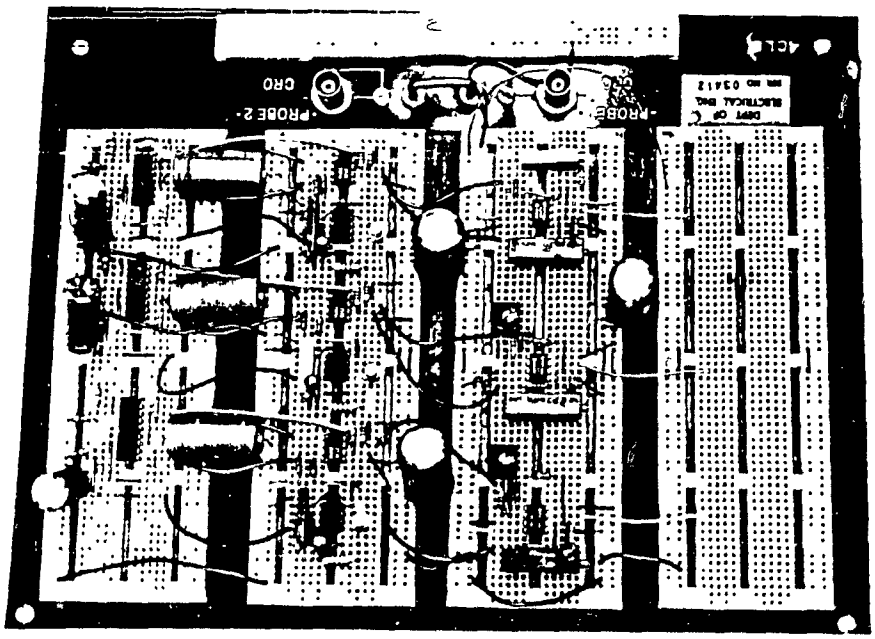


Fig.C.3 Three Phase Capacitor Voltage Measurement Circuit (CVM).

All the remaining control circuits were made on printed circuit boards. Fig.C.4 shows the photograph of the three phase voltage reference generator (VRG).

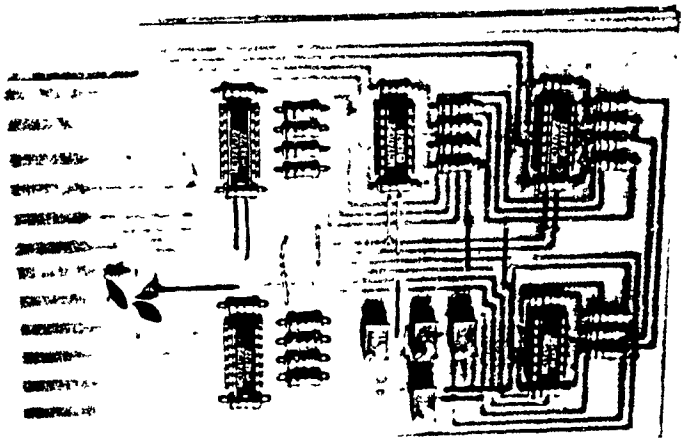


Fig.C.4 Three Phase Voltage Reference Generator (VRG).

Fig.C.5 is the photograph of the printed circuit board that contains the single phase circuits for voltage comparison (VC) and base drive logic (BDL) respectively. After modification, the PC-board of Fig.C.5 contains MVC and MBDL circuits.

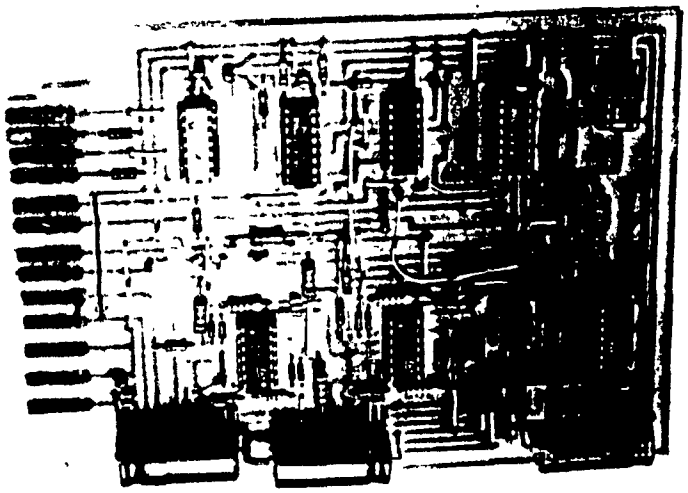


Fig.C.5 Single Phase Circuit Board Containing the VC and BDL (MVC and MBDL) circuits.

Fig.C.6 and C.7 show the photographs of modular arrangement of one leg of the single phase H-bridge of the converter. It includes two power switches, snubber circuits and two base drive units.

The base drive units are on the left side PC board (Fig.C.6). The right side PC board contains the snubber circuits. The power switches are located in between the two PC-boards on the heat sinks. Power connections are on the right of Fig.C.7.

Fig.C.8 shows the photograph of the modular arrangement for single phase H-bridge. Finally, Fig.C.9 shows the photograph of the complete three phase converter.

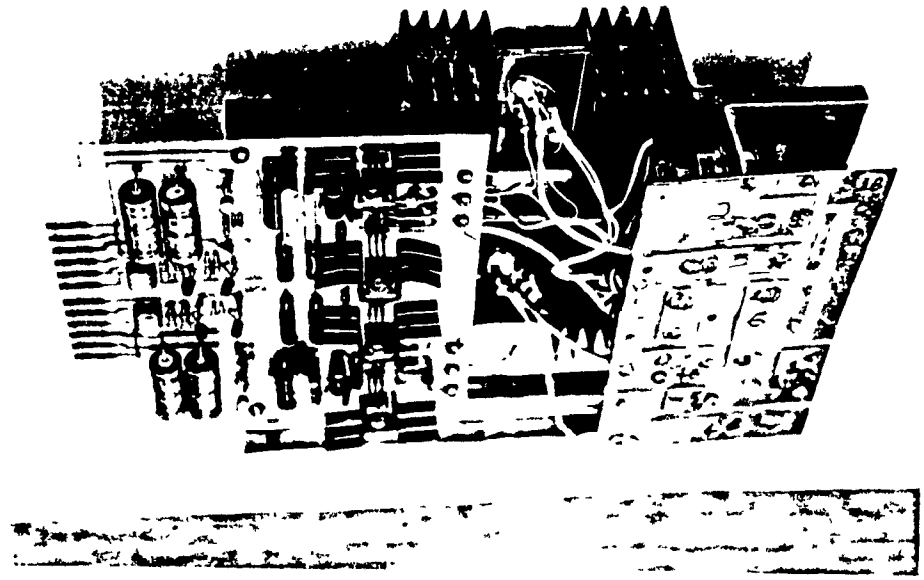


Fig.C.6 Modular arrangement for one leg of the H-bridge.

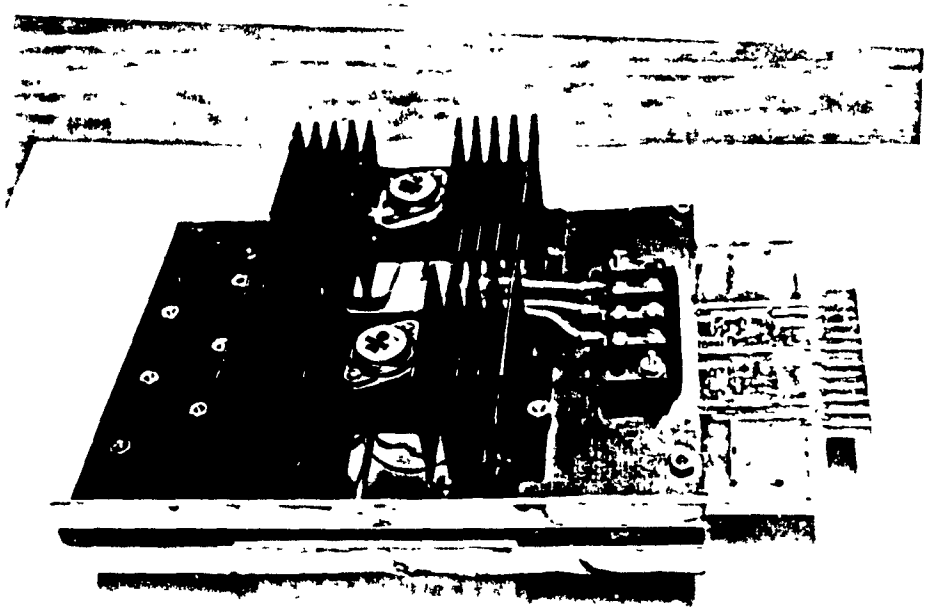


Fig.C.7 Power Transistors and Power Connections.

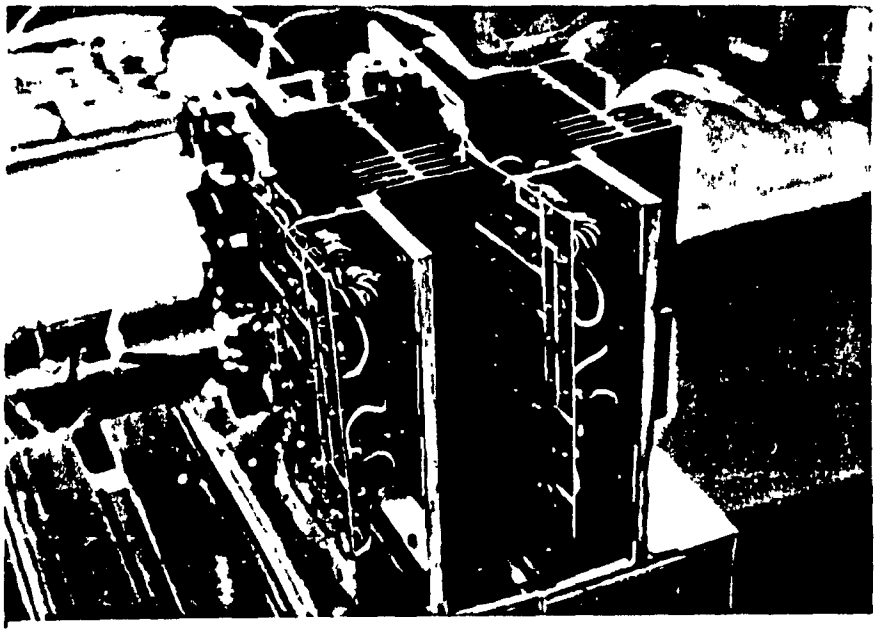


Fig.C.8 Modular arrangement for one phase H-bridge.

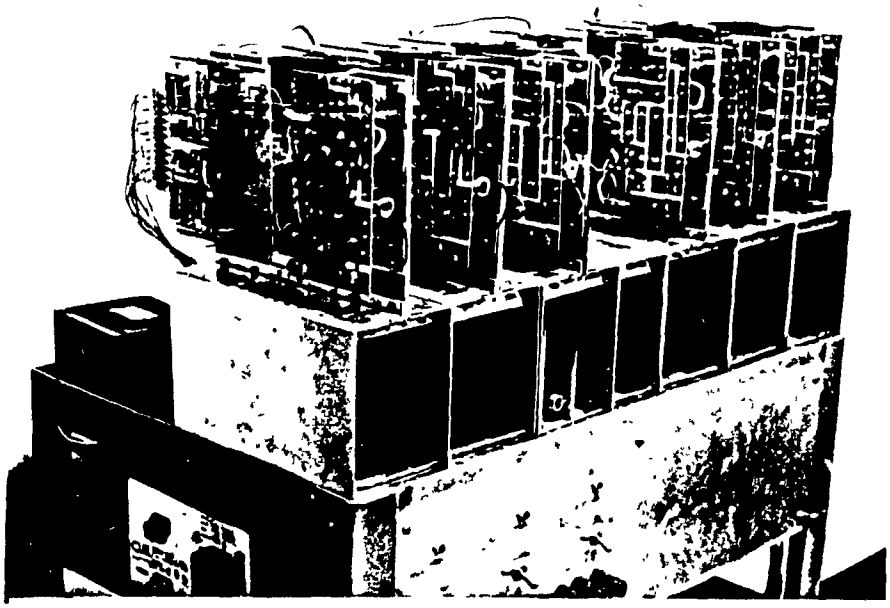


Fig.C.9 Complete Three-Phase Delta Modulated PWM Converter.